CMOS Front-End Circuits in 45-nm SOI Suitable for Modular Phased-Array 60-GHz Radios

by

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Author's Declaration

I hereby declare that I am the sole author of this thesis. This is a true copy of the thesis, including any required final revisions, as accepted by my examiners.

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Abstract

Next Fifth-generation (5G) wireless technologies enabling ultra-wideband spectrum availability and increased system capacity can achieve multi-gigabit/s (Gbps) data rates suitable for ultra-high-speed internet access around the 60-GHz band (i.e., Wi-Gig Technology). This mm-wave band is unlicensed and experiences high propagation power losses. Therefore, it is suitable for short-range communications and requires antenna arrays to satisfy the link budget requirements. Half-duplex reconfigurable phased-array transceivers require wideband, low-cost, highly integrated front-end circuits such as bilateral RF switches, low-noise/power amplifiers, passive RF splitters/combiners, and phase shifters implemented in deep sub-micron CMOS.

In this dissertation, analysis, design, and verification of essential CMOS front-end components are covered and fabricated in GlobalFoundries 45-nm RF-SOI CMOS technology. Firstly, a fully-differential, single-pole single-throw (SPST) switch capable of high isolation in broadband CMOS transceivers is described. The SPST switch realizes better than 50-dB isolation (ISO) across DC to 43 GHz while maintaining an insertion loss (IL) below 3 dB. Measured RF input power for 1-dB compression (IP_{1dB}) of the IL is +19.6 dBm, and the measured input third-order intercept point (IIP3) is +30.4 dBm (both assuming differential inputs at 20 GHz). The prototype has an active area of 0.0058 mm^2. Secondly, a single-pole double-throw (SPDT) switch is implemented using the SPST concept by using a balun to convert the shared differential path to a single-ended antenna port. The SPDT simulations predict less than 3.5-dB IL and greater than 40-dB ISO across 55 to 65 GHz frequency band. An IP_{1dB} of +21 dBm is expected from large-signal simulations. The prototype has an active area of 0.117 mm^2. Thirdly, a fully-differential switched-LC topology adopted with slow-wave artificial transmission line concept, and phase inversion network is described for a 360° phase shift range with 11.25° phase resolution. The average IL of the complete phase shifter is 5.3 dB with less than 1-dB rms IL error. Furthermore, the IP_{1dB} of the phase shifter is +16 dBm. The prototype has an active area of 0.245 mm^2. Lastly, a fully-differential, 2-stage, common-source (CS) low-noise amplifier (LNA) is developed with wideband matching from 57.8 GHz to 67 GHz, a maximum simulated forward power gain of 20.8 dB, and a minimum noise figure of 3.07 dB. The LNA consumes 21 mW and predicts an OP_{1dB} of 4.8 dBm from the 1-V supply. The LNA consumes an active area of 0.028 mm^2.

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Dedication

Dedicated to my mother, Eatimad Bayoumi, the most supportive and caring woman on Earth. May God rest her in peace, forgive her sins, and bring her to paradise.

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Abbreviations

5G	Fifth-Generation
BC	Body Contact
BEOL	Back-End-of-Line
BER	Bit-Error Rate
BPSK	Binary Phase Shift Keying
CMOS	Complementary Metal-Oxide-Semiconductor
CPW	Coplanar Waveguide
dBm	decibel-milliwatts
DL	Down-Link
EIRP	Effective Isotropic Radiated Power
FB	Floating Body
FET	Field Effect Transistor
Gbps	Giga-bit per second
HBT	Heterojunction Bipolar Transistors
I-Q	Inphase-Quadrature
IF	Intermediate Frequency
IL	Insertion Loss
IP3	Third-Order Intercept Point
ISM	Industrial, Scientific and Medical
ISO	Isolation

LNA	Low-Noise Amplifier
LOS	Line-of-Sight
LSB	Least Significant Bit
MAG	Maximum Available Gain
MC	Monte Carlo
MCS	Modulation and Coding Schemes
MIMCAP	Metal-Insulator-Metal Capacitor
mm-Wave	Millimeter-Wave
NF	Noise Figure
NLOS	Non-Line-of-Sight
OFDM	Orthogonal Frequency-Division Multiplexing
PA	Power Amplifier
PAPR	Peak-to-Average Power Ratio
PS	Phase Shifter
PVT	Process, Voltage, and Tempreture
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
RF	Radio-Frequency
RL	Return Loss
rms	root-mean-square
SC	Single Carrier
SiGe	Silicon-Germanium
SNR	Signal-to-Noise Ratio
SOC	System-on-Chip
SOI	Silicon-on-Insulator

SPDT	Single-Pole, Double-Throw
SPST	Single-Pole, Single-Throw
SRF	Self-Resonance Frequency
TL	Transmission Line
UE	User Equipment
UL	Up-Link
VGA	Variable Gain Amplifier
VNA	Vector Network Analyzer
VNCAP	Vertical-Natural Capacitor
WiFi	Wireless Fidelity
WiGig	Wireless Gigabit
WLAN	Wireless Local-Area Network

Chapter 1

Introduction

Among the requirements for next-generation wireless systems (for both cellular and wireline access), achieving multi-gigabit/sec (Gbps) data rates is a priority. Millimeter-wave (mm-wave) wireless technologies have been proposed to achieve this goal using the 28-GHz [1] and 60-GHz [2] bands. The use of mm-wave bands for next-generation wireless systems offers the advantage of ultra-wide bandwidth (i.e., 10% to 20% bandwidth as a fraction of the operating frequency f_o), spectrum availability, and increased channel capacity.

These benefits come at the expense of greater system complexity, particularly in terms of radio-frequency (RF) front-end circuit and antenna design. However, recent advancements in mm-wave wireless systems [3] [4] have the potential to reduce cost in volume production that could overcome these challenges. The 60-GHz band is selected for this work because data communication in this band is standardized by the IEEE 802.11ad protocol [5].

1.1 Multi-Gbps Motivation

The emerging fifth-generation (5G) of wireless technology includes, but is not limited to, advances in higher data transfer speeds, greater capacity, and lower latency. Moreover, it should be capable of supporting billions of connected devices and *things* via the internet. Figure 1.1 shows trends driving the next generation of radio applications. The supported data rates range from a few kilobits/sec (i.e., less than 1 Mbps) for ultra-low-energy machine communications, to multi-Gbps rates (i.e., greater than 5 Gbps), targeting ultra-high-data-rate access. To fulfill the demand for a wide range of data rates, a wideband operation is required from the radio circuits.

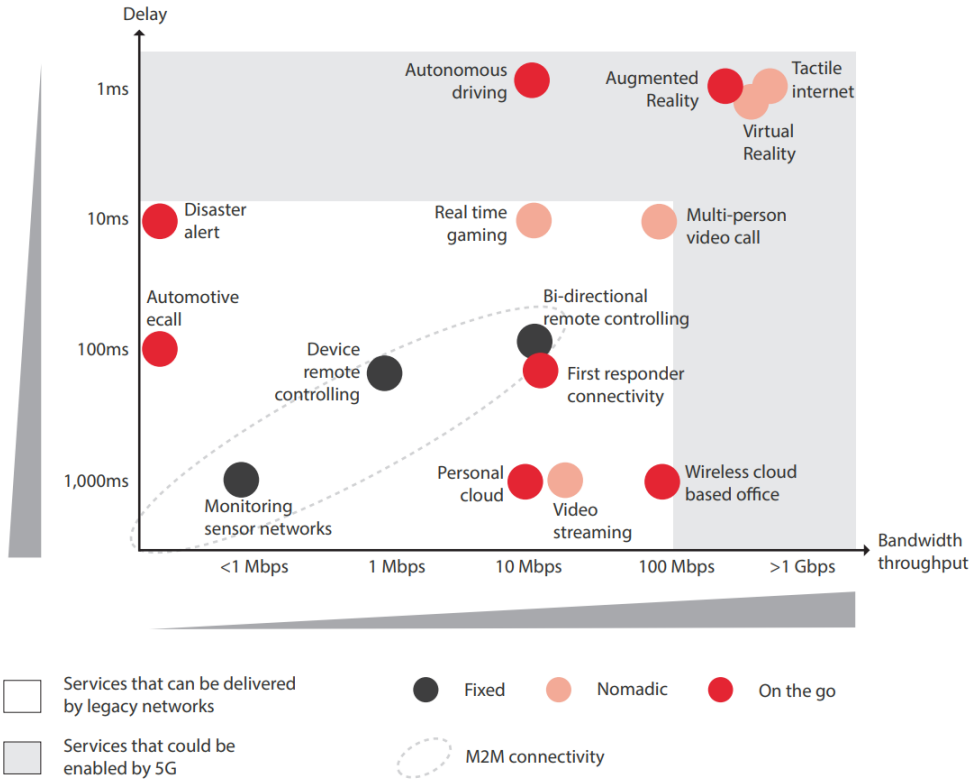


Figure 1.1: 5G technology potential application trends with target data rates/latency [6]

Figure 1.2 shows the wireless spectrum for the established standards as well as potential mm-wave applications. The ISM bands in the sub-6 GHz range offer relatively narrow bandwidth compared to the mm-wave frequency bands above 10 GHz. Multi-Gbps data rates can be achieved when mm-wave technologies are employed. Furthermore, mm-wave frequencies enable the reduction of hardware size as the frequency increases, opening up the possibility of higher system integration on a silicon chip. A silicon system-on-chip (SoC) for 60-GHz WiFi (known as WiGig) is an enabling technology to fulfill the high data-rate demand, that could migrate to other frequency bands targeting other applications if it proves feasible. As silicon technologies evolve, larger bandwidth/data-rates can be achieved beyond 100 GHz (sub-THz range) enabling new wireless technologies (e.g., radio imaging) and applications in the future.

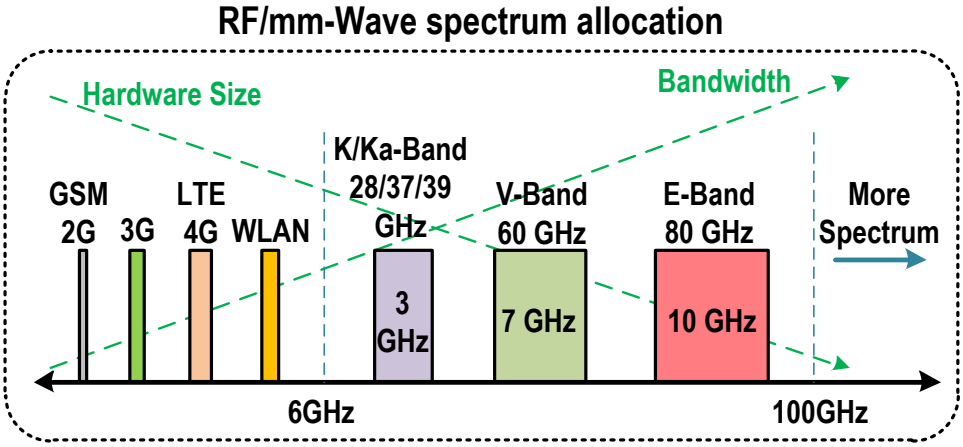


Figure 1.2: RF/mm-wave spectrum allocations [7]

1.2 mm-Wave Path-Loss Propagation Models

Figure 1.3 [8] shows sea-level atmospheric losses across different mm-wave frequencies. The atmospheric absorption of energy at different microwave frequencies [9] [10] provides transmission windows suitable for long- and short-range communications. The window at 35 GHz has been adopted for commercial satellite communications. Other windows at 90/140/220/345 GHz are also suitable for long-range communications. On the other hand, there are attenuation peaks located at 60/119/183/325 GHz, which constrain communication in these bands to only short distances. Unfortunately, some of these frequency windows are not available for commercial use. However, the 60-GHz band (57-66 GHz), also known as V-band, is unlicensed and provides standardized wideband channels (via IEEE 802.11ad) that can be used for Gbps data rates.

Figure 1.4 shows an evaluation of different path loss models from [11] for the 60-GHz band in urban areas assuming that the user equipment (UE) height is 1.5 m. The non-line-of-sight (NLOS) transmission loss is higher than that of line-of-sight (LOS) transmission. It can be seen that the breakpoints in the path loss models depend on the base station (BS) height. In the 60-GHz band, the T-R separation is limited to 10 m to 100 m. Thus, the propagation loss for this band is around 100 dB to 140 dB.

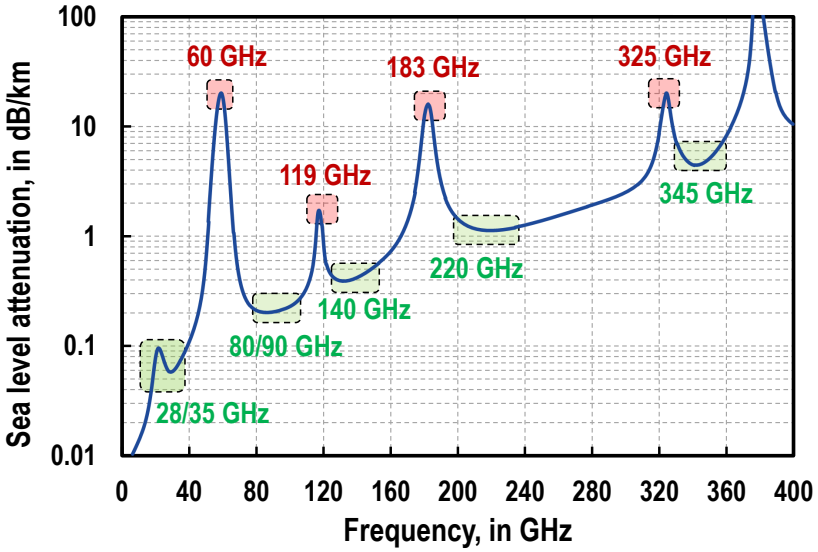


Figure 1.3: Sea level atmospheric absorbtion across different microwave frequencies

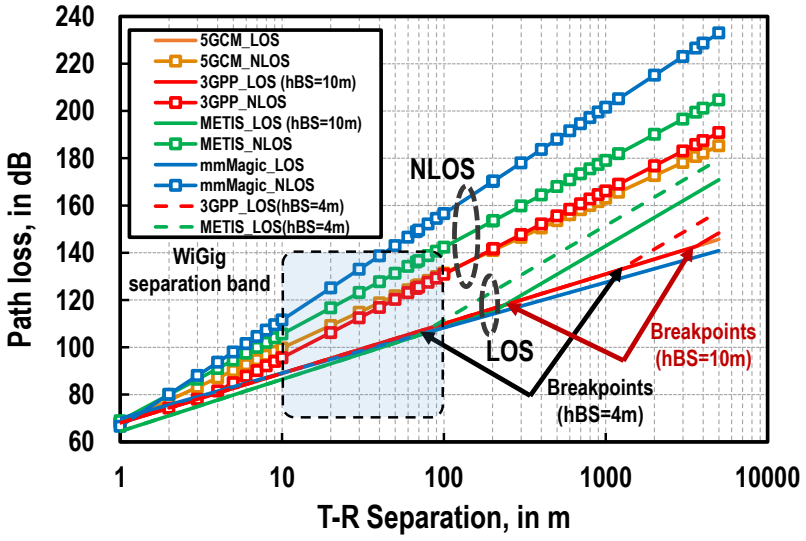
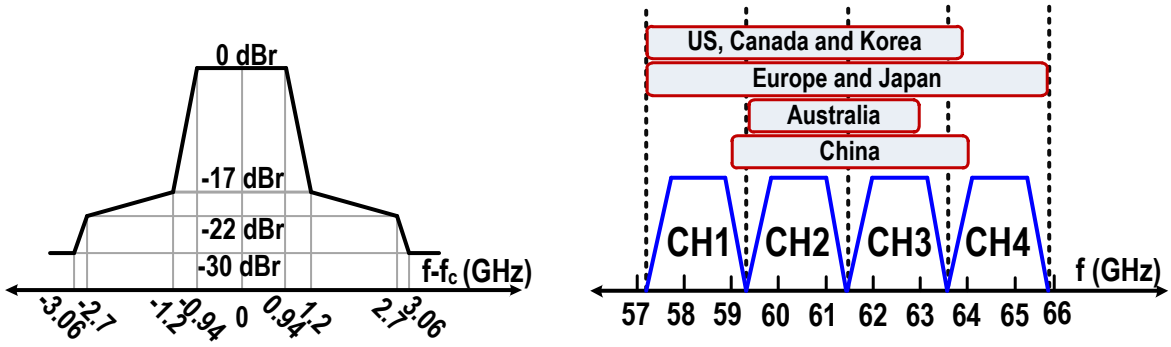


Figure 1.4: 60-GHz omnidirectional path loss models for urban micro-cell communication



(a) (b)

Figure 1.5: WiGig spectrum specifications: (a) transmit mask (b) global spectrum allocaion

1.3 60-GHz Spectrum Requirements

The objective of this work is to investigate the feasibility of implementing hardware in silicon for use in the 60-GHz band. The performance of the circuits should satisfy the requirements of the wireless standard. The IEEE 802.11ad protocol standardizes the unlicensed 60-GHz band for wireless local-area networks (WLAN) [5]. Since the propagation loss at mm-wave frequencies is relatively high (see Fig. 1.4), multi-Gbps data rates (e.g., for multimedia applications) are only achieved for short-range communication (i.e. 10 m to 100 m Tx-Rx separation). Hence, the deployment of several wireless access points in a given area (i.e., route diversity) is essential for a reliable link.

Figure 1.5 [5] shows the spectral mask for a transmitter. The maximum allowed bandwidth is 2.4 GHz, however, the flat bandwidth at peak output is 1.88 GHz. The unlicensed bands available globally are shown in Fig. 1.5(b). A total of 4 channels are defined between 57 GHz and 66 GHz. In North America, 7-GHz of unlicensed spectrum is available between 57 GHz to 64 GHz.

A total of 25 different modulation and coding schemes (MCS) are supported in the standard, consisting of single-carrier (SC) and orthogonal frequency-division multiplexing (OFDM) signaling schemes. The SC modulation schemes are BPSK, QPSK, 16- and 64-QAM. The maximum achievable data rates from the different MCS range from 27.5 Mbps up to 6.75 Gbps.

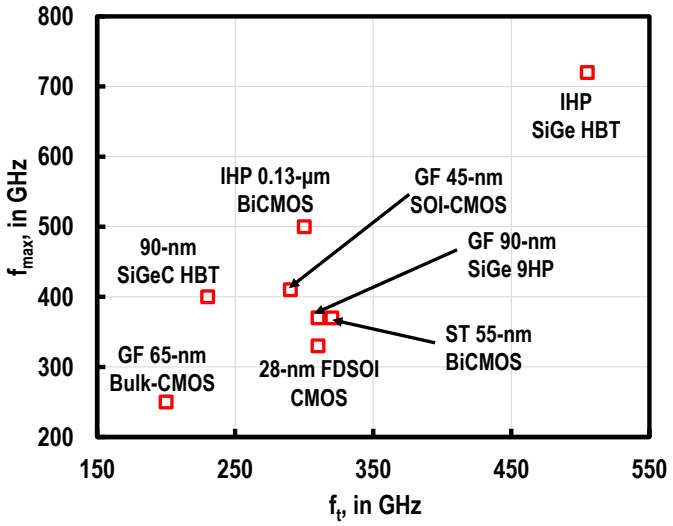


Figure 1.6: Recent comparison between potential mm-wave silicon technologies

1.4 Technology Selection for mm-Wave Applications

Among different silicon technologies available, high RF/mm-wave performance with a margin for process, temperature and supply (PVT) variations is essential for the development of reliable integrated mm-wave wireless transceivers for communications. Figure 1.6 shows peak f_t and f_{max} values [12–19] for technologies developed for RF/mm-wave applications in the last 10 years. A detailed survey of RF/mm-wave/THz silicon technologies is found in [15].

Technology choice depends on factors such as: 1) extrinsic versus intrinsic RF device performance, 2) intrinsic device performance and reliability, 3) passive components, and 4) cost in volume production. Firstly, f_t and f_{max} do not scale linearly with transistor gate length. Moreover, the extrinsic versus intrinsic RF device performance is highly dependent on device geometry and back-end-of-line (BEOL) metal stack options that are available. Theoretically, smaller feature-length provide higher f_t/f_{max}, however, this is not completely true when switching from 45-nm SOI-CMOS to 28-nm FDSOI (see Fig.1.6).The reported values are measured at the device terminals including metal connections from the substrate to the top metal layer. Transistor performance is impaired by the increased interconnect parasitic capacitance. Secondly, bipolar technologies provide higher transconductance (g_m) values and breakdown voltages when compared to CMOS counterparts. For example, the IHP 0.13-μm BiCMOS and SiGe HBT (see Fig.1.6) report superior performance when compared to other technologies. Thirdly, the BEOL stacks of BiCMOS technologies are

focused on RF/mm-wave applications, as a result, they deliver high-Q passive elements and low-loss interconnects, where high integration densities are not required. Advanced CMOS technologies are focused on digital applications, which require high integration density of interconnected transistors in a given area. Finally, BiCMOS technologies require additional masks [15] compared to CMOS technologies. They are not suitable for high-volume low-cost integration due to increased fabrication cost, which is a significant advantage for CMOS technologies. Moreover, CMOS technologies are attractive when integrating low-power RF/mm-wave circuits with digital/analog/mixed-signal sub-systems on the same system-on-chip (SoC). 45-nm SOI-CMOS provides a balance between optimized mm-wave performance (i.e., higher f_t and f_{max} compared to Bulk-CMOS) and the possibility for high integration density. Thus, it provides a low-power low-cost mm-wave/mixed-signal platform for wireless handsets.

GlobalFoundaries^{TM} started the development of 45-nm SOI-CMOS for 5G mm-wave applications in 2008 [13]. This technology aims at decreasing the intrinsic parasitic capacitance of active devices as well as providing thick copper and aluminum BEOL metal interconnects for high-frequency applications. Also, a high-resistivity substrate option reduces the energy loss of high-Q passive components compared to bulk-CMOS technologies. This technology features high f_{max} values when compared to 65-nm bulk-CMOS and 28-nm FDSOI (see Fig.1.6) which makes it attractive for CMOS PA design, with stacking capability, for high output power/gain/efficiency. Lower-loss interconnects and higher-f_t transistors enable the development of high-performance low-noise amplifiers (LNAs) [20] through lower minimum noise figure (NF_{min}) at mm-wave frequencies. Moreover, high-resistivity substrates and low-R_{ON} devices enable lower insertion loss [21] and higher linearity with device stacking [21], which enable improved performance from transmit-receive (T/R) switches integrated in CMOS for use at mm-wave frequencies.

Figure 1.7 shows a cross-section of the 45-nm SOI-CMOS technology used in this work. This process offers partially-depleted floating body N-FET and P-FET devices with a 40-nm gate length, and body-contacted N-FET and P-FET devices with a 56-nm gate length. The transistors are fabricated over a 225-nm thick buried oxide layer that isolates the active area from the substrate. The technology offers 2 substrate resistivities: 13.5 Ω.cm and 900 Ω.cm. The buried oxide capacitance to the substrate is 4× to 7× lower than that for bulk-CMOS [22], thus parasitic energy losses to the substrate (e.g., from integrated passive components such as inductors, capacitors, and resistors) are expected to be lower than seen in bulk-CMOS technologies. Detailed technology characterization for mm-wave applications (i.e., active and passive circuits characterized at mm-wave frequencies) can be found in [23].

This technology offers several metal stack options, the adopted ones are only shown in

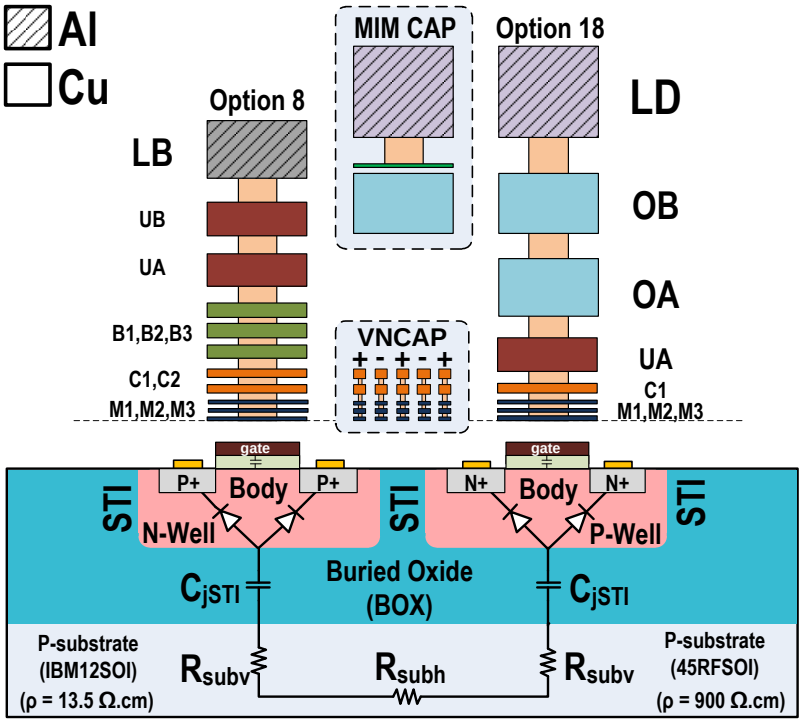


Figure 1.7: Cross section of GF 45-nm SOI-CMOS with supported metal stack options and passives

the figure. Option 8 provides 11 metal layers. The 10 lower layers are copper while the top layer is aluminum, all connected through tungsten vias. Option 18 offers 8 metal layers. However, the top aluminum metal layer is thicker and higher above the substrate than that the top metal of option 8.

The 45-nm SOI-CMOS technology also offers some BEOL (back-end-of-line) passive elements. The most important of these structures are VNCAP (Vertical Natural Capacitors) and MIMCAP (Metal-Insulator-Metal Capacitors). Both are shown in Fig. 1.7. VNCAPs are usually used for high-density decoupling capacitors, in the picofarad (pF) range, to isolate DC biasing pads from RF signals. Moreover, they are also used to create small-area RF capacitors using the C1 metal layer (shown in Fig. 1.7). Stacking between metals M1 and C1 is available, depending on the capacitance value. MIMCAPs (shown in Fig. 1.7) provide high-Q capacitors (larger than 100) provided that the capacitance value remains below 50 fF.

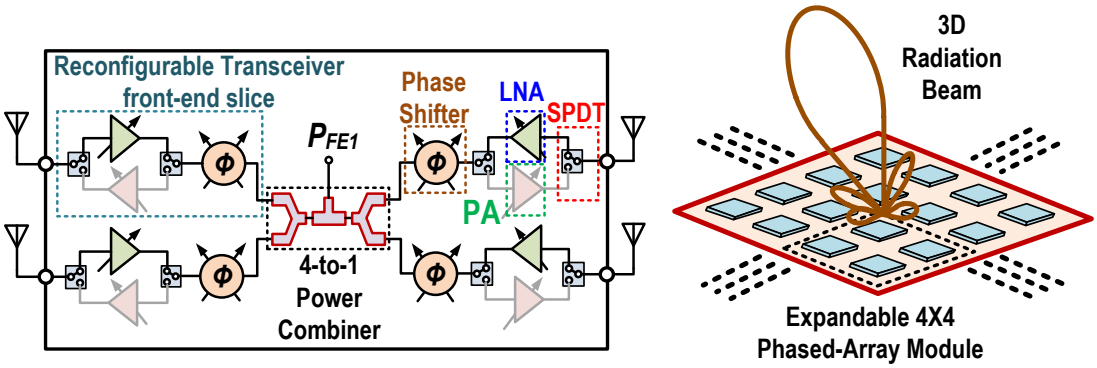


Figure 1.8: Block diagram of the 2 × 2 RX beamformer front-end developed in this work

1.5 State-of-the-Art Performance Summary

Figure 1.8 shows the block diagram of a 2 × 2 receive beamformer front-end that can be used to implement an expandable N × N phased-array module. Typically, the beamformer consists of several reconfigurable RF front-end slices. Each front-end slice is connected to a single antenna in the antenna array, as shown in the figure. The front-end slice is comprised of a single-pole, double-throw (SPDT) switch, a low-noise amplifier (LNA) in the receive path, a power amplifier (PA) in the transmit path, a second SPDT for double-path combining, and a 360° phase shifter. The output power of each of the front-end slices is then combined using a 2-to-1 power combiner. This combining is repeated multiple times in a higher-order beamforming front-end. Power amplifier design is not addressed in this thesis. However, SPDT switches, LNAs, and phase shifters are developed for the receive mode of the front-end shown in Fig. 1.8.

A single-pole, double-throw switch is usually placed at the interface between the antenna, the transmitter PA, and the receiver LNA (see Fig. 1.8). Ideally, the switch should provide low insertion in the ON state (IL, close to 0 dB) and infinite isolation (ISO) in the OFF state. An insertion loss (IL) of 1-3 dB, isolation (ISO) of less than 30 dB, and an input 1-dB compression power level (P_{1dB}) of 5-10 dBm are the typical performance benchmarks which are obtained from a survey of mm-wave SPDT switches reported in the literature [24–26]. However, most designs don't provide sufficient isolation between the LNA and PA. The air interface (see Fig. 1.4) predicts that at least 50 dB between Tx/Rx paths is required to prevent signal feedthrough. Also, the capability to handle input signal compression is not high enough to cope with the power generated from a 60-GHz CMOS PA (i.e., larger than 15 dBm [27]). Cascoding (i.e., stacking) more devices should increase P_{1dB} and isolation but increases the insertion loss.

An electronic phase shifter is needed before the power splitter/combiner of the beamformer (see Fig. 1.8) to enable beamforming in a phased-antenna array. This work focuses on digital passive shifters because of several of their performance advantages. They have linear, uniform performance when compared to analog phase shifters [28]. Also, a single phase shifter may be shared between PA and LNA of a single transceiver slice because a passive circuit is reciprocal, hence saving silicon area. Moreover, from a literature study (see Chapter 2 for a literature survey), passive phase shifters are attractive as they consume no DC power. One drawback, however, is that they consume a relatively bigger physical area (i.e., 2 to 4 times as estimated from [29]). Another disadvantage is that cascading more stages to achieve higher phase resolution deteriorates the insertion loss. IL and group delay flatness are other important metrics and determined by the root-mean-square (rms) error of both IL and group delay. An rms error of less than 1 dB and 10 ps is recommended for IL and group delay, respectively. The IL rms error determines the amount of variable-gain amplification needed to compensate for gain deviation across phase states, accordingly, there will be area/power overhead. Phase rms error is important to be kept low (i.e., smaller than 1 LSB of phase resolution) to prevent excessive signal dispersion across frequency when retrieving the received modulated signal. Moreover, based on a literature survey [28, 30], 360° passive phase shifters realize an IL of 6-10 dB in both directions and matching bandwidth of greater than 10 GHz across the 60-GHz band. One drawback in literature is that P_{1dB} is limited to 10 dBm, which might be a problem for the transmitter if a preamplifier driver is used before the phase shifter.

Low-noise amplifiers (LNAs) are required just after the SPDT switch to amplify the received signal with minimum noise overhead, and also suppress the noise added by the subsequent stages in the receiver chain. Linearity is less critical at 60 GHz as the received signal power is as low as -60 dBm or even lower. Potential interferers may increase the received power level up to -30 dBm (based on a 50-dBm maximum EIRP transmitter located at less than 10 m separation with an 80-dB path loss). The LNA noise figure (NF) should be as low as possible, as it dominates the receiver noise figure. LNA gain should be sufficient to amplify the received signal, but not high enough to saturate the following stages in a receiver chain. DC power consumption should be low enough to conserve battery energy without sacrificing gain and NF. Designs reported recently at 60 GHz in CMOS [23, 31, 32] realize a NF of at least 4 dB, a forward gain of greater than 10 dB, and power consumption of less than 20 mW. Input return loss (RL) achieved is larger than 10 dB for greater than 7-GHz bandwidth.

1.6 Thesis Organization and Contribution

The thesis work is divided into 4 stages. Firstly, in Chapter 4, SPST/SPDT switch prototypes are developed targeting high isolation greater than 50 dB and high linearity greater than 15 dBm with low IL below 3 dB and minimal physical area. Secondly, in Chapter 5, a highly-linear, reciprocal 360° passive phase shifter is developed targeting low IL/group delay rms error of less than 1 dB and 10 ps, respectively, across states and bandwidth. Thirdly, in Chapter 6, a low-power LNA is developed targeting a low NF of 3 dB and a high gain of 20 dB. Finally, in Chapter 7, a reconfigurable front-end slice is designed by cascading SPDT switch, LNA, SPDT switch, and phase shifter with some modifications on the system-level for best performance. Chapter 8 highlights a concluding summary and future work.

The target performance benchmarks of the individual blocks are summarized in Table 1.1. The target benchmarks are deduced from literature performance at the 60 GHz band and several iterations of electromagnetic (EM) simulations done for the technology devices and components including BEOL metal layers. Throughout the design iterations, the active area of the fabricated prototypes is kept as small as possible. Also, It should be noted that the circuit techniques used in this work are transferable across frequency bands and different technology nodes.

Table 1.1: Target Performance Benchmarks for the Phased-Array Front-End

	SPDT switch	Phase Shifter	LNA
Frequency Band (GHz)		57 - 64	
I/O Return Loss (dB)		> 10	
Gain (dB)	—	—	> 20
Insertion Loss (dB)	< 3	6±1	—
Isolation (dB)	> 50	6±1	> 30
Phase Shift (°)	180	360 (11.25° steps)	0
Noise Figure (dB)	3	6±1	3
Input P_{1dB} (dBm)	> 15	> 15	> -15
Power Consumption (mW)	0	0	< 20

Chapter 2

Background and Literature Review

This chapter highlights the basic principles of designing front-end circuits, that can be used in a phased-array transceiver. These principles include circuit topologies for single-pole, double-throw switches (SPDT), low-noise amplifiers (LNA), and phase shifters (PS). Additionally, implementations from recent literature in different CMOS technology nodes are covered across several mm-wave frequencies including the 60-GHz band. Finally, a performance comparison from literature is presented, which highlights performance trade-offs with respect to circuit parameters.

2.1 CMOS Single-Pole, Double-Throw (SPDT) Switch

An RF switch is a device that controls the passage of signals in an electronic circuit. The switch can take two states, either ON, by allowing the signal to pass, or OFF by blocking the signal. The switch can be implemented in CMOS, as shown in Fig. 2.1 [33], or using other technologies (e.g., PIN diodes [34] and RF-MEMS [35]). The CMOS switch (Fig. 2.1) isolates the DC control from the RF signal path and consumes no DC power.

The performance of different switch designs is defined by a set of metrics. Insertion loss (IL) is defined by the attenuation of the transmit/receive (T/R) switch between input and output ports. Isolation (ISO) is defined by the leakage from the input of the T/R switch to ports other than the desired output. From Eqns. 2.1, 2.2 for a series switch, and Eqns. 2.3, 2.4 for a shunt switch [33], IL and ISO are determined by the switch small-signal parameters R_{ON} and C_{OFF} of series and shunt switches. Linearity is determined by the

(a) (b)

Figure 2.1: CMOS RF switch types (a) series switch (b) shunt switch

third-order intercept point (IIP3 or OIP3) for third-order inter-modulation distortion. The -1 dB compression of the IL (IP_{1dB}) determines the input power, where IL drops by 1 dB.

$$IL = 20.log_{10}\left(1 + \frac{R_{ON}}{2Z_o}\right), \tag{2.1}$$

$$ISO = 10.log_{10}\left(1 + \frac{1}{[4.\pi.f_o.C_{OFF}.Z_o]^2}\right), \tag{2.2}$$

$$IL = 10.log_{10}\left(1 + [\pi.f_o.C_{OFF}.Z_o]^2\right), \tag{2.3}$$

$$ISO = 20.log_{10}\left(1 + \frac{Z_o}{2R_{ON}}\right), \tag{2.4}$$

where R_{ON} is the drain to source resistance of the RF switch in the ON state, C_{off} is the drain to source capacitance in the OFF state, f_o is the frequency of operation, and Z_o is the source impedance (normally 50 Ω).

2.1.1 Switch DC I-V characteristics

Figure 2.2 shows the $I_D - V_{DS}$ characteristics of an NMOS switch. The switch operates in the linear resistive region, where V_{DS} should be biased close to 0 V. The slope of the I-V curve across 0 V should be maximized (i.e., R_{ON2} is smaller than R_{ON1}) to minimize the IL of the switch, which is realized when V_{GS} is maximized. R_{ON} of a MOS transistor is given by Eqn.2.5 [36]:

$$R_{ON} = \frac{1}{\mu C_{ox}(W/L)(V_{gs} - V_{th})}. \tag{2.5}$$

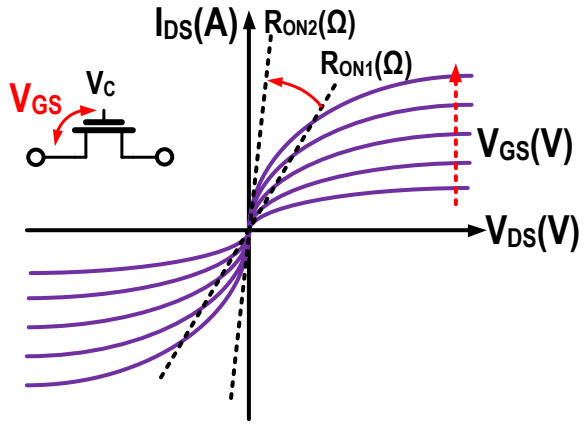


Figure 2.2: DC I-V characteristics of an NMOS switch

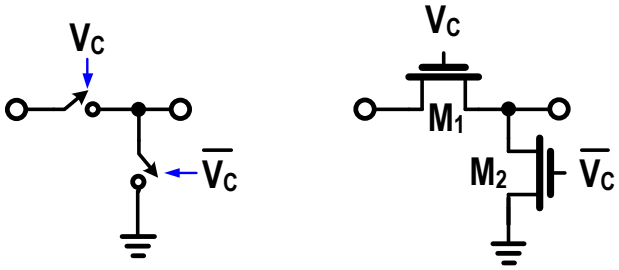


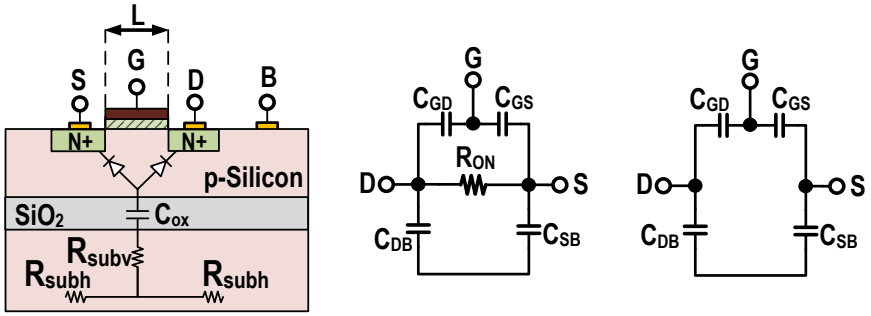
Figure 2.3: Series-shunt switch realization (a) ideal switch (b) practical CMOS switch

2.1.2 Series-Shunt Switch Realization

A single series CMOS switch is designed for low ON resistance (R_{ON}), while ISO decreases between ports. Fig. 2.3 shows the basic series-shunt SPST topology of a CMOS switch for increased isolation. During ON state, transistor M_1 is biased ON, while M_2 is biased OFF. Conversely, during the OFF state, M_1 is biased OFF, while M_2 is biased ON.

2.1.3 CMOS SOI Switch Small-Signal Model

An N-FET RF switch implemented in SOI-CMOS (i.e., only NMOS transistors shown) with simplified small-signal models for switch ON and OFF states is shown in Fig. 2.4 (neglecting the effects of C_{ox} and R_{sub}). In the ON state, IL is minimized by decreasing R_{ON}, which is controlled by the channel width W when the minimum channel length L is chosen. During the OFF state, the maximum ISO between ports is realized if the



(a) (b) (c)

Figure 2.4: Analog/RF switch technology in RF-SOI CMOS (a) cross-sectional view, (b) ON-state small-signal circuit model, and (c) OFF-state small-signal circuit model

lateral parasitic capacitances of the transistor, i.e., C_{gs}, C_{gd}, C_{sb}, and C_{db} are minimized. This is achieved by minimizing W (again, assuming L is minimum). Power handling of conventional bulk-CMOS switches is limited by the turn-ON voltage of parasitic diodes embedded in the substrate [21]. The substrate is isolated from the transistor channel and body by a buried SiO_2 layer in SOI technologies (see Fig. 2.4), which enables larger RF power compression capability compared to bulk-CMOS devices. Cascoding (or stacking) of switches may be used to further increase compression limits by lowering the RF swing across each transistor in the chain. However, power handling is traded-off against increased IL when multiple transistors are connected in series.

2.1.4 Conventional mm-Wave SPDT Implementations

Figure 2.5 shows a traveling wave SPDT switch [37]. The authors firstly introduce a low-loss broadband SPDT switch from 50 GHz to 94 GHz. The design incorporates microstrip transmission lines with distributed shunt switches for each path. When the transistors are OFF, the RF signal propagates across the low IL lines. When the transistors are ON, the RF signal is grounded. The T junction is a quarter-wave ($\lambda/4$) line, such that the shorted switch path appears open circuit at the common node. One drawback is the large physical area of the transmission lines compared to MOS transistors. The design realizes an IL of 2.7 dB, and an ISO of 29 dB in 90-nm bulk-CMOS using floating body switches. The input compression point IP_{1dB} of the switch is 15 dBm.

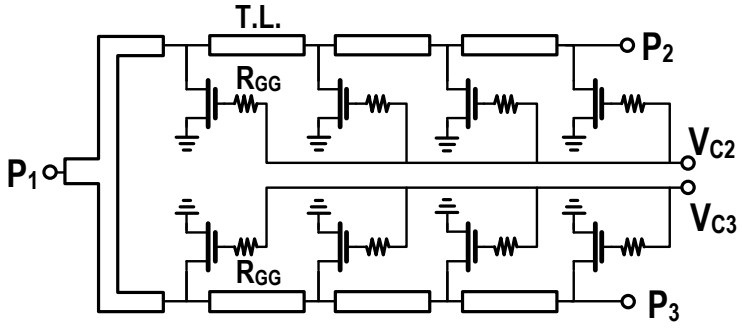


Figure 2.5: Low-loss traveling-wave switch schematic

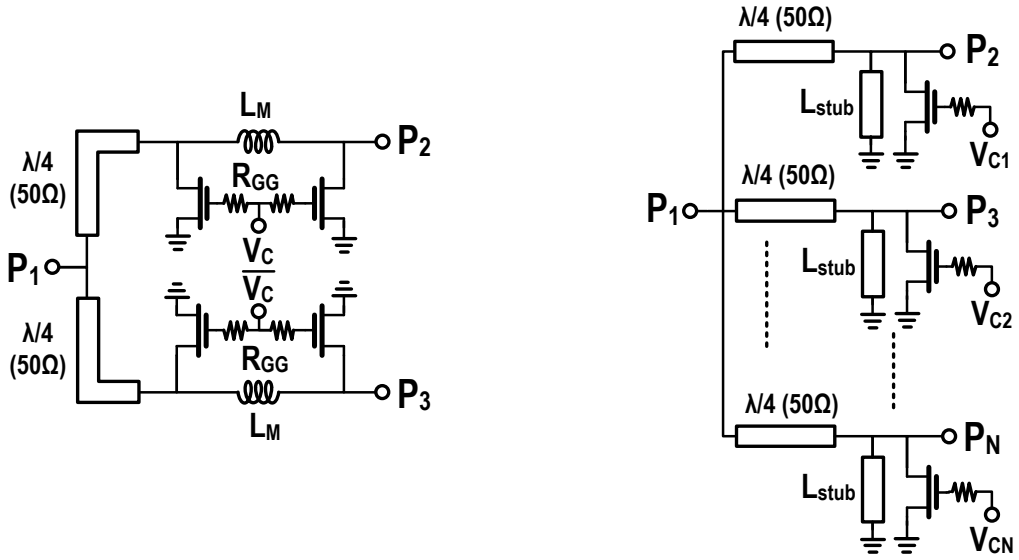


Figure 2.6: $\lambda/4$-based shunt switch circuit schematics with lumped matching network: (a) SPDT and (b) SP4T

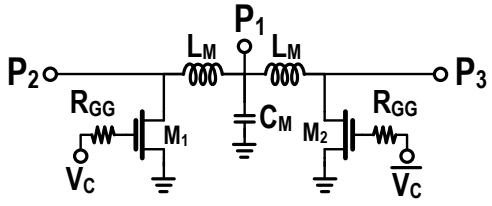


Figure 2.7: L-C matching SPDT circuit schematic

Table 2.1: Performance Summary of mm-Wave CMOS SPDT Switch from Literature

FOM	[37]	[38]	[39]	[40]	[41]	[22]
Tech.	130nm CMOS	130nm CMOS	90nm CMOS	130nm CMOS	90nm CMOS	45nm-SOI CMOS
Topology	Travelling Wave Switch	Shunt-Shunt & $\lambda/4$ stubs	Shunt & $\lambda/4$ stubs	Lumped Matching Network	Asymm & $\lambda/4$ Shunt Network	Series Shunt
Freq. (GHz) (S_{11}>10dB)	50-94	45-67	50-70	57-66	50-67	DC-60
IL (dB)	<3.3	<2.5	1.5(min.)	<2	1.9	<2.5
ISO (dB)	>27	>30	>25	>21.1	>38	>25
Input P_{1dB} (dBm)	15	13	13.5	10	10	7.1
Supply Voltage (V)	0/1.2	0/1.2	0/1.2	0/1.2	0/1.2	0/1
Active Area (mm^2)	0.24	0.125	0.27	0.02	0.3	0.04

Fig. 2.6 shows another two CMOS switch topologies introduced in [38]. Design A (see Fig. 2.6a) is an SPDT switch incorporating $\lambda/4$ junction for isolation. During ON-state, ports P_2 or P_3 are matched to 50 Ω using both the lumped inductor L_M and the OFF-state parasitic capacitance of the shunt switches. Design B (see Fig. 2.6b) is a single-pole, four-throw (SP4T) using the $\lambda/4$ lines for each path, however, it comprises 50 Ω stubs. During ON-state, the shunt stubs resonate with the parasitic capacitance of the OFF-switch for 50-Ω matching.

Both designs are fabricated in 0.13 μm-CMOS realizing wideband return loss (RL) of -10 dB across 50 GHz to 70 GHz. The IL realized for design A and B is 2 dB and 2.3 dB, respectively. The achieved isolation for design A and B is 32 dB and 22 dB, respectively. The simulated compression point P_{1dB} is 14 dBm, which is lower than the typical power (i.e., 20 dBm) generated from a 60-GHz power amplifier in 45-nm SOI-CMOS.

Another SPDT switch topology is developed in [40]. The switch matching is based on lumped components for shunt MOS switches at each port as shown in Fig. 2.7. Using LC matching saves significant physical area when compared to distributed matching. The design achieves an IL of 2 dB, an ISO of 21 dB, and a matching bandwidth of 57 to 66 GHz in 130-nm bulk-CMOS. Although, the active area of the prototype is small, the measured compression point of 10 dBm, which is low to handle the power generated from CMOS

power amplifiers.

A performance summary between several mm-wave SPDT switch designs is shown in Table 2.1. All the examples listed in the table are based on the circuit implementations discussed in this section.

2.2 CMOS Active/Passive Phase Shifter

A phase shifter is defined by an electronic circuit whose output signal is a phase-shifted version of the input signal. The ideal scattering matrix of a reciprocal phase shifter is given by Eqn. 2.6:

$$S = \begin{bmatrix} 0 & Ae^{-j\phi} \\ Ae^{-j\phi} & 0 \end{bmatrix}, \tag{2.6}$$

where A is the phase shifter gain. For an active phase shift, the gain is greater than unity. Whereas, for a passive phase shift, the gain is smaller than unity. ϕ is the amount of added phase shift to the signal.

The phase shift is changed by a control signal, where A is ideally constant. However practical implementations experience gain variations. The active phase shifters are non-reciprocal networks. Generally, phase shifters can be divided into 2 main categories based on the control scheme. Continuous phase shift achieves a phase range of between ϕ_{min} and ϕ_{max}. The control voltage or current signal changes between V_{min} to V_{max} or I_{min} to I_{max}, respectively. This phase shifter can potentially achieve infinite phase resolution within the operating dynamic range. Digital phase shifters realize a discrete phase range of $(\phi_1, \phi_2, ..., \phi_N)$, which is based on a digitally controlled signal. The achievable phase resolution is determined by the phase shift order $(log_2 N)$.

Eqn. 2.6 is modified for practical phase shifters by Eqn. 2.7, where both gain and phase change over frequency. Constant phase shifters have a constant phase variation across frequency for a specific phase state. Whereas, true-time delay phase shifter has a linear phase shift variation with frequency (i.e., $\phi = \omega.\Delta t$).

$$S = \begin{bmatrix} 0 & A(\omega)e^{-j\phi(\omega)} \\ A(\omega)e^{-j\phi(\omega)} & 0 \end{bmatrix}. \tag{2.7}$$

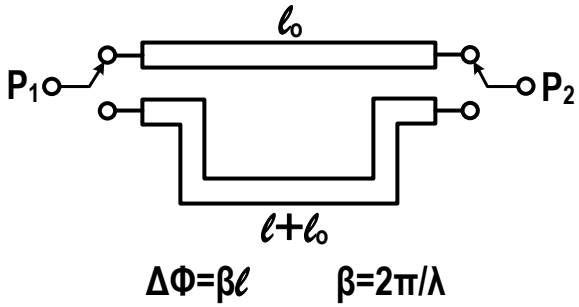


Figure 2.8: Switched-line phase shifter

2.2.1 Passive Phase Shift Techniques

Fig. 2.8 shows a basic phase shifter, where the RF signal is allowed to propagate between two switched transmission lines of different lengths. As a result, two different time delays are realized. The transmission line of length (l_o) realizes a phase shift of ($\phi = 2\pi l_o/\lambda$). So, the phase shift realized between the 2 transmission lines is given by:

$$\Delta\phi = \frac{2\pi l}{\lambda}, \tag{2.8}$$

where l is the difference of length between the transmission lines.

This topology is inherently wideband. However, there are several drawbacks. Single switched-line phase shifter incorporates two SPDT switches, which introduce losses to the phase shifter. When the phase shift order increases, the total switch losses increase significantly. Additionally, practical transmission lines with different lengths have different losses, which introduce insertion loss (IL) deviation. Also, IL deviation increases with phase shift order, as more stages are cascaded. This topology consumes a large physical area, especially when cascading more stages.

Fig. 2.9 shows the loaded-line phase shift architecture [42]. The phase shifter incorporates a quarter-wave ($\lambda/4$) line loaded with lumped inductors and capacitors on both ends. The phase shift, in terms of the susceptance B, is given by:

$$\Delta\phi = tan^{-1}\left(\frac{1}{BZ_o} - \frac{BZ_o}{2}\right). \tag{2.9}$$

By changing the termination susceptance B, the phase shift is changed. However, the input and output reflection coefficient increases with B [42]. As a result, realizing a higher-

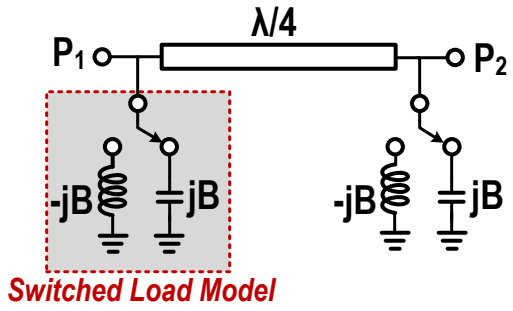


Figure 2.9: Loaded-line phase shifter

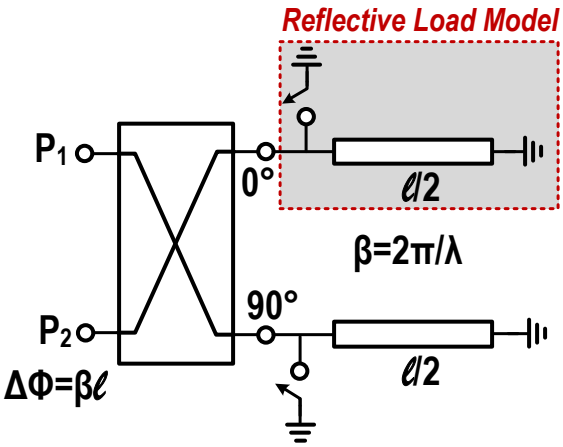


Figure 2.10: Reflection-type phase shifter

order phase shift degrades the port matching. Hence, the load-line phase shifter is limited to small phase steps.

The reflection-type phase shifter generic topology is shown in Fig. 2.10, where the switched reflective loads can be implemented using lumped L-C elements, as in [43], or digitally controlled varactors, as in [44]. The phase shifter consists of a quadrature coupler, and 2 transmission lines of length $l/2$ each, where l is the length corresponding to the required phase shift. The RF signal is inserted from P_1 and divided equally at the transmission line ports. If the switches are shorted to the ground, the signals are reflected, and then combined at P_2. If the switches are open, the signals travel back and forth by $l/2$. This is equivalent to a travel length of l and then combined at P_2 with a phase shift equivalent to that in Eqn. 2.8.

Isolation between input and output ports is a key advantage of using the reflection-

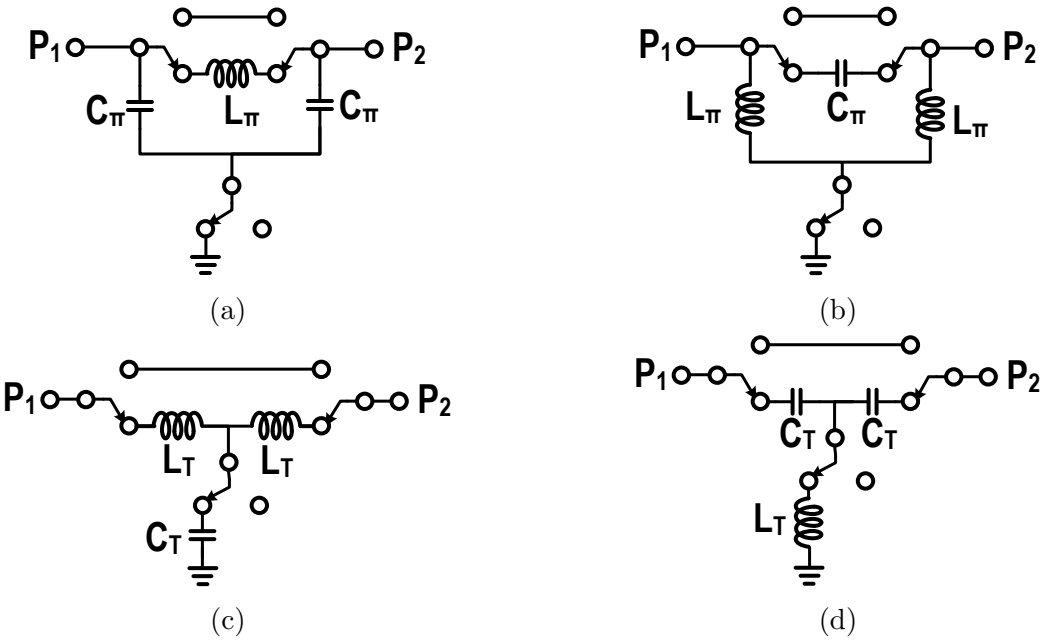


Figure 2.11: Switched L-C phase shift circuits: (a) low-pass Π-model, (b) high-pass Π-model, (c) low-pass T-model, and (d) high-pass T-model

type phase shifter. Otherwise, the reflection-type and switched-line phase shifters share the same features.

Fig. 2.11 shows 4 different types of lumped-LC phase shift. Three passive components can realize a phase shift in the range of $-90 \leq \phi \leq 90$. The corresponding values for each network for a matching impedance Z_o at frequency ω_o are listed below [45]:

Low-pass π-network:

$$L_\pi = \frac{Z_o sin|\phi|}{\omega_o}, \tag{2.10a}$$

$$C_\pi = \frac{tan|\phi/2|}{\omega_o Z_o}, \tag{2.10b}$$

High-pass π-network:

$$L_\pi = \frac{Z_o}{\omega_o tan|\phi/2|}, \tag{2.11a}$$

$$C_\pi = \frac{1}{\omega_o Z_o sin|\phi|}, \tag{2.11b}$$

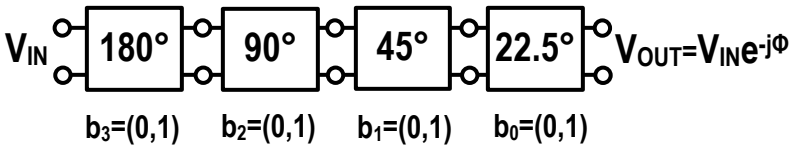


Figure 2.12: Digital phase shifter block diagram

Low-pass T-network:

$$L_T = \frac{Z_o tan|\phi/2|}{\omega_o}, \tag{2.12a}$$

$$C_T = \frac{sin|\phi|}{\omega_o Z_o}, \tag{2.12b}$$

High-pass T-network:

$$L_T = \frac{Z_o}{\omega_o sin|\phi|}, \tag{2.13a}$$

$$C_T = \frac{1}{\omega_o Z_o tan|\phi/2|}. \tag{2.13b}$$

The phase shift can be realized by switching between a by-pass state, and a phase shift state as shown in Fig. 2.11. Also, the phase shift may be realized by switching between high-pass to low-pass networks. The total amount of phase shift required is 360° for a phased-array transceiver, so cascading more phase shift stages is required with different phase steps.

Fig. 2.12 shows the block diagram of a complete digital phase shifter. The number of cascaded stages is determined by the phase resolution of the system requirements. The first stage phase shift starts by 180°, and then each subsequent stage phase shift is divided by 2 (i.e., 90°, 45°, ...). The phase shift of the output signal is given by Eqn. 2.14. Cascading more stages increases the insertion loss of the overall phase shifter, as it incorporates cascaded lossy switches.

$$\phi = (180°.b_3) + (90°.b_2) + (45°.b_2) + (22.5°.b_1). \tag{2.14}$$

2.2.2 Active Phase Shifter Topologies

Active phase shifters involve active circuitry that performs the phase shift and adds gain to the input signal. The most common active phase shift topology is the vector modulated

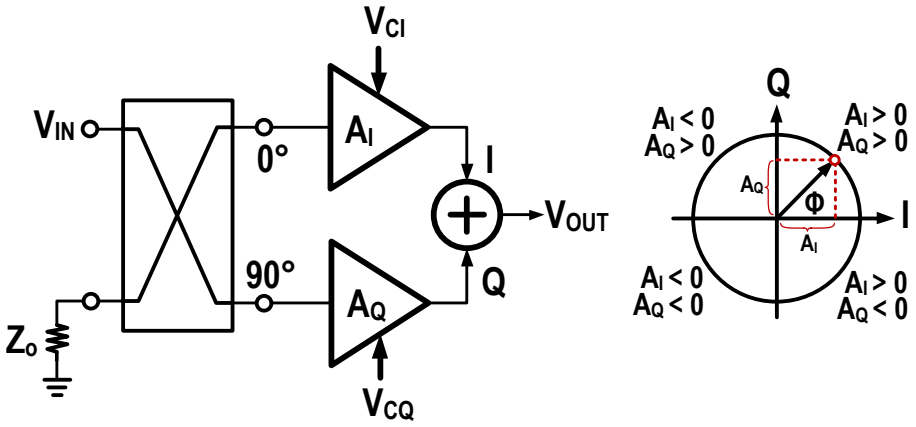


Figure 2.13: Vector-modulated phase shift block diagram

phase shifter shown in Fig. 2.13 [46]. The phase shifter consists of three main building blocks. Firstly, the 90° quadrature coupler generates in-phase and quadrature vectors. Each vector is then amplified by a separate variable gain amplifier (VGA), which can be continuously or digitally controlled. Finally, the modulated vectors are combined to generate the final phase-shifted signal. The phase shift added to the output signal is determined by the gain of the VGAs. The phase rotation of the shifter is shown in Fig. 2.13.

Expressions for the magnitude and phase of the output signal are given by :

$$|V_{out}| = \frac{v_{in}}{\sqrt{2}}(|A_I|^2 + |A_Q|^2), \tag{2.15}$$

$$\phi = \begin{cases} tan^{-1}\left(\dfrac{|A_Q|}{|A_I|}\right), & A_I \geq 0, A_Q \geq 0 \\ 180 - tan^{-1}\left(\dfrac{|A_Q|}{|A_I|}\right), & A_I < 0, A_Q \geq 0 \\ 180 + tan^{-1}\left(\dfrac{|A_Q|}{|A_I|}\right), & A_I < 0, A_Q < 0 \\ -tan^{-1}\left(\dfrac{|A_Q|}{|A_I|}\right). & A_I \geq 0, A_Q < 0 \end{cases} \tag{2.16}$$

From Eqn. 2.16, any phase between 0° and 360° can be generated according to A_I and A_Q values. Moreover, from a system perspective, a flat gain response is required across all states. As a result, A_I and A_Q have to be appropriately scaled in each quadrant

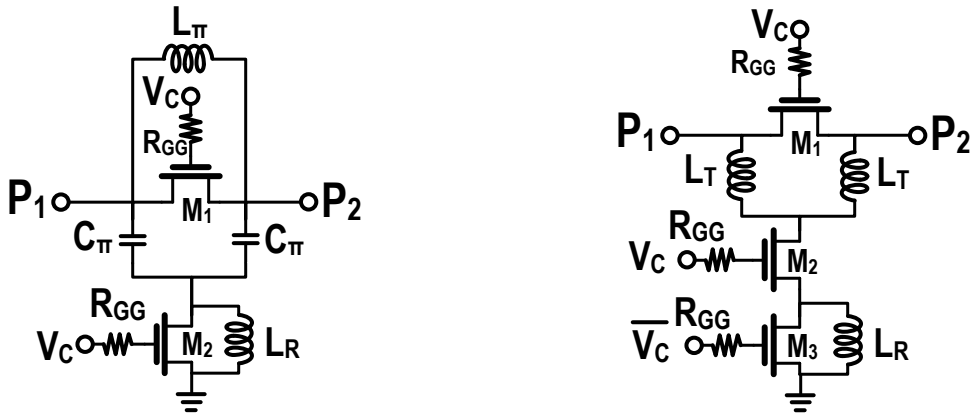


Figure 2.14: CMOS switched L-C low-pass/by-pass implementations: (a) π-model and (b) T-model

to maintain the constant magnitude of the output vector for all states. For example, the minimum gain value of I and Q vectors in the 4^{th} quadrant when $\phi = -45$ is $A_I = A_Q = A$, so $|V_{out}| = \sqrt{2}A$. When $\phi = 0$, $A_I = \sqrt{2}A$ and $A_Q = 0$ to preserve the same magnitude for the output signal. So A_I and A_Q should change by up to 3 dB from their lowest values. The value of A determines the overall gain of the phase shifter.

This topology can achieve small phase resolution and can be calibrated against process variations. The physical area is more compact when compared to other topologies. Moreover, the VGA maximum gain compensates for the I-Q generator and the output combiner losses. As a result, the phase shifter can achieve a power gain of greater than 0 dB. The phase shifter circuit is unilateral and consumes DC power for using VGAs, which limit the phase shifter linearity.

2.2.3 CMOS mm-Wave Phase Shifter Implementations

The published work on CMOS phase shifters is focused on switched topologies as in [47–50], and active vector-modulated phase shifters as in [29, 51–53]. In this section, basic implementations are covered, as each design involves a different circuit design.

Fig. 2.14 shows two implementations for switched LC phase shifters, that are commonly used in literature. Fig. 2.14a shows the π-model switched low-pass by-pass 1-cell phase shifter. When M_1 is open and M_2 is closed, the input is phase-shifted by C_π and L_π, while

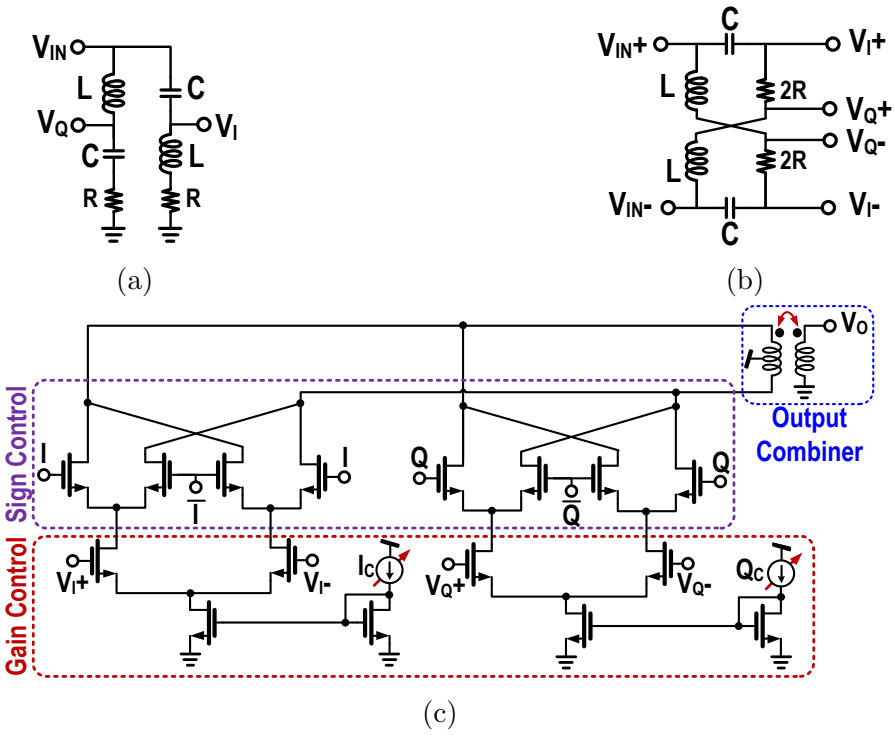


Figure 2.15: Vector-modulation phase shift circuit schematics: (a) single-ended lumped I-Q signal generator, (b) differential lumped I-Q signal generator, and (c) variable-gain amplifiers with linear power combining

L_R is shorted to ground. When M_1 is closed and M_2 is open, the input signal is bypassed to the output port through M_1, while L_R creates an open circuit resonance with the C_{off} of switch M_2.

Fig. 2.14b shows a similar technique for T-model switched low-pass by-pass 1-cell phase shifter. In [48], the authors claim that the T-model architecture provides better group delay than the π-model architecture, especially at mm-wave frequencies.

Active phase shifters involve several signal conditioning blocks to generate the phase states. Fig. 2.15a shows the passive I-Q single-ended signal generator based on the RLC network. Fig. 2.15b shows the fully-differential version of the I-Q generator, which is commonly used with differential VGAs for vector modulation. The analysis of the I-Q generator is covered in [52].

Basic CMOS implementation of VGAs is shown in Fig. 2.15c. The input signals are fed from a differential I-Q generator to the common-source differential pairs. The gain is

controlled by the current mirror of the tail current source (see gain control in Fig. 2.15c). Quadrant selection is controlled by switching 4 common-gate amplifiers, according to the in-phase and quadrature vector signs (see Sign Control in Fig. 2.15c). The generated vectors are then current combined using an output balun (see output combiner in Fig. 2.15c).

A performance comparison is shown in Table 2.2. from recent literature, that includes active and passive design circuits across different mm-wave bands in several technology nodes.

Table 2.2: Performance Summary of mm-Wave Phase Shifters from Recent Literature

	[47][1]	[48][1]	[49][1]	[50][1]	[52][1]	[53][1]
Tech.	45nm-SOI CMOS	90nm CMOS	65nm CMOS	40nm CMOS	0.13μm SiGe BiCMOS	90nm CMOS
Topology	Switched HP/LP Network	Switched T-LP Network	Switched HP/LP Network	Switched HP/LP Network	Active Vector Sum +LNA	Active Vector Sum
Freq. (GHz) (S_{11}<-10dB)	60-67	57-64	57-66	22-36	60-80	58.8-64.3
Phase Resolution (°)	45	11.25	22.5	45	22.5	22.5
RMS Phase Error (°)	<3	<10	<5.5	<12.8	<9.1	<10
Gain (dB)	-6	>-18	-8.7±1.7	-5.6±0.5	<14.7	<1.1
RMS Gain Error (dB)	<1.3	<1.8	<1.17	<0.6	1.3	<1.6
Input P_{1dB} (dBm)	6	—	7.4	<12	-27[3]	-9.8±0.8
Supply Voltage (V)	0/1	0/1.2	0/1	0/1	3	1.8
DC Power (mW)	0	0	0	0	108/34.8[4]	19.8
Active Area (mm^2)	0.3[2]	0.34	0.092	0.132	1.06[5]	0.61[5]

Based on the performance summary shown in Table 2.2, several design aspects are concluded. Firstly, achieving smaller phase resolution from passive phase shifters realizes

[1]All designs realize 360° phase shift range
[2]Estimated from the chip photo
[3]Measured at 70 GHz
[4]Consumed by the phase shifter only
[5]Including pads

higher insertion loss (IL). The design in [47] realizes an IL of 6 dB for a phase resolution of 45°, while [49] achieves an IL of 8.7 dB for a 22.5° phase resolution. The IL is even worse for a phase shift resolution of 11.25° as reported in [48]. Secondly, the linearity quantified by IP_{1dB} of passive phase shifters is better than active phase shifters as shown in Table 2.2. Although an LNA is used before the phase shifter of [52], which is limiting the phase shifter compression. The IP_{1dB} of a stand-alone active phase shifter as in [53] is still smaller than -5 dBm. Thirdly, active phase shifters consume DC power as shown in Table 2.2, which is not suitable for low-power applications. This can be seen from [52], which consumes a total DC power of 108 mW. Moreover, the design of [52] consumes a larger physical area when compared to that of [53], since [52] incorporates transmission lines for matching, while [53] uses lumped component matching.

2.3 CMOS Low-Noise Amplifiers

A low-noise amplifier (LNA) is a 2-port electronic circuit, that amplifies an input RF signal with minimal noise contribution. The LNA is placed after the receiving antenna to suppress the noise contribution of later blocks in a receiver chain. Since the signal-to-noise-ratio (SNR) of the received signal is not sufficient for back-end baseband processing, low noise contribution, and high power gain are required.

This section discusses low-noise amplifier (LNA) analysis and design in CMOS technologies. Multistage microwave amplifier design theory is discussed in detail in [54], however, the design procedure is summarized. Also, CMOS technology limitations for amplifier design are presented, to understand the frequency-dependent parameters that affect noise, gain and, matching. Literature circuit architectures are investigated, to understand the development of LNAs across different frequencies. Finally, mm-wave LNA designs from recent literature are presented, as an overview for the state-of-the-art mm-wave LNAs.

2.3.1 Gain and Noise Analysis

From the microwave theory perspective, a microwave amplifier is a 2-port network that has a maximum available gain (G_{max}) between its input and output ports. This gain is only achieved at specific source and load impedance, which are called optimum source and load impedance for maximum power transfer $Z_{S,og}$, $Z_{L,og}$, and are given by:

$$Z_{S,og} = R_{S,og} + jX_{S,og}, \tag{2.17}$$

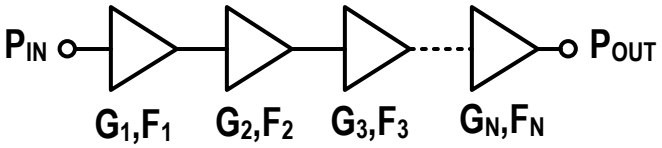


Figure 2.16: Cascaded amplifier gain and noise factor model

$$Z_{L,og} = R_{L,og} + jX_{L,og}. \tag{2.18}$$

When $Z_S = Z^*_{S,og}$ and $Z_L = Z^*_{L,og}$, maximum power transfer at the input and output ports is realized, when the amplifier is stable. The stability factor (μ) of a 2-port amplifier is calculated by [54] :

$$\mu = \frac{1 - |S_{11}|^2}{|S_{22} - (S_{11}S_{22} - S_{21}S_{12})S^*_{11}| + |S_{21}S_{12}|} > 1, \tag{2.19}$$

where S_{11}, S_{12}, S_{21}, and S_{22} are the S-parameters of the amplifier.

Matching networks are needed at the input and output ports to convert the port impedances to their optimum values. It should be noted that impedance variations at source and load decrease the gain from its maximum. Moreover, the resistive losses of the matching networks decrease the overall amplifier gain.

The LNA noise factor definition, in terms of the noise parameters of the amplifier, F_{min} and R'_n, is given by [20]:

$$F = F_{min} + \frac{R'_n}{G_S}[(G_S - G_{S,on})^2 + (B_S - B_{S,on})^2], \tag{2.20}$$

where $G_{S,on}$ and $B_{S,on}$ are the source optimum noise conductance and susceptance required for minimum noise factor matching, respectively.

The complex optimum noise impedance is given by:

$$Z_{S,on} = R_{S,on} + jX_{S,on}. \tag{2.21}$$

The amplifier's noise factor is maintained at F_{min}, when $Z_S = Z^*_{S,on}$, which is called minimum noise factor matching.

Fig. 2.16 shows the cascaded amplifier gain and noise factor model. Assuming all amplifiers are matched to their corresponding optimum noise and gain impedance, the overall gain and noise factor (i.e., Friis formula [55]) are given by:

$$G_{tot} = G_1.G_2.....G_N, \tag{2.22}$$

$$F_{tot} = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + ... + \frac{F_N - 1}{G_1 G_2 ... G_{N-1}}. \tag{2.23}$$

Eqn. 2.23 shows that the total noise factor is dominated by the noise factor of the first stage, as long as G_1 is sufficient to suppress the generated noise of later amplifier stages.

2.3.2 CMOS Technology Gain and Noise Parameters

The MOSFET devices of 45-nm SOI-CMOS technology are used in a tuned amplifier configuration in this work as common-source or cascode configurations. As a result, the effect of circuit parameters on both gain and noise figure should be understood. This analysis is a good starting point for circuit design refinement using computer simulators.

A simplified reactively-tuned circuit analysis for common-source or cascode amplifiers is found in [33], where the final amplifier power gain is given by :

$$G_p(f) = \frac{f_T^2}{4 f_o^2} \frac{r_o}{R_g + R_s} = \frac{f_{max}^2}{f_o^2}, \tag{2.24}$$

where r_o is the output resistance of the MOSFET device, $R_g + R_s$ is the total input resistance seen by the device at the gate terminal, f_t is the transit frequency of the technology, f_{max} is the frequency where the uni-lateral gain of the device is unity, and f_o is the operating frequency.

Choosing a well-developed technology for mm-wave applications (i.e., f_t is $4\times$ to $6\times$ f_o) is essential for the development of CMOS amplifiers for high gain.

The minimum noise factor of a MOSFET device is given by [20] :

$$F_{min} = 1 + 2 g_m (r_{gg} + r_{Lg}) \gamma (\frac{f_o}{f_t})^2 + 2 \frac{f_o}{f_t} \sqrt{g_m (r_{gg} + r_{Lg}) \gamma (1 + g_m (r_{gg} + r_{Lg}) \gamma (\frac{f_o}{f_t})^2)}, \tag{2.25}$$

This equation can further be simplified given the following conditions :

If $g_m (r_{gg} + r_{Lg}) \gamma (\frac{f_o}{f_t})^2 \ll 1$, then :

$$F_{min} \approx 1 + 2g_m(r_{gg} + r_{Lg})\gamma(\frac{f_o}{f_t})^2 + 2\frac{f_o}{f_t}\sqrt{g_m(r_{gg} + r_{Lg})\gamma}, \tag{2.26}$$

If $g_m(r_{gg} + r_{Lg})\gamma(\frac{f_o}{f_t})^2 \gg 1$, then :

$$F_{min} \approx 1 + 4g_m(r_{gg} + r_{Lg})\gamma(\frac{f_o}{f_t})^2, \tag{2.27}$$

where r_{gg} and g_m are the device gate resistance and transconductance, respectively, γ is the excess drain channel noise parameter, which is technology-dependent.

From Eqns. 2.26, 2.27, $r_{gg} + r_{Lg}$, g_m, and f_t are circuit design parameters, which can be adjusted for low noise operation. g_m and f_t of the MOSFET transistor can be adjusted using the DC bias point setting, and the aspect ratio of the transistor. Minimizing r_{gg} is done by splitting the device into smaller multiple fingers M, and connecting each finger using double-gate contacts. 1-μm wide transistor unit is reasonable for most CMOS processes. The new gate resistance, as a result, is given by [56] :

$$r_{gg} = \frac{1}{12}\frac{\rho_{sh}W}{ML}, \tag{2.28}$$

where ρ_{sh} is the gate sheet resistance in $\Omega/\square$, W and L are the device width and length, respectively.

The optimum current density $(\frac{I_{DS}}{W})_{opt}$ is used instead of the drain current I_{DS} [33] to bias the transistor for F_{min}. The effective voltage of the MOSFET transistor, in terms of the current density, is given by [36] :

$$V_{eff} = V_{GS} - V_{TN} \approx \sqrt{\frac{2L}{\mu_n C_{ox}}\frac{I_{DS}}{W}}, \tag{2.29}$$

where μ_n, C_{ox} and V_{TN} are the carrier mobility, gate oxide capacitance per unit area, and the threshold voltage of the MOSFET device.

The optimum source noise impedance $Z_{S,on}$, in terms of device parameters, is given by [20, 33] :

$$R_{S,on} = \frac{1}{\omega_o M(C'_{gs} + C'_{gd})}\sqrt{\frac{r'_{gg}g'_m}{\gamma}}, \tag{2.30}$$

$$X_{S,on} = \frac{1}{\omega_o M(C'_{gs} + C'_{gd})}, \tag{2.31}$$

where r'_{gg}, g'_m, C'_{gs}, and C'_{gd} are the gate resistance, transconductance, gate-to-source capacitance and gate-to-drain capacitance of a unit-size transistor, respectively.

$R_{S,on}$ can be adjusted to the source impedance (i.e., 50 Ω) using the number of fingers M, without changing the optimum current density required for the minimum noise factor. As the technology scales down, $R_{S,on}$ increases. As a result, the device width should be increased to set $R_{S,on}$ at 50 Ω, given the transistor is biased to its optimum current density. As a result, there is a trade-off between decreasing noise figure and minimizing power consumption. Moreover, increasing transistor width may degrade gain and noise figure due to the Miller effect, especially at mm-wave frequencies.

As frequency scales up for a specific technology node, the number of fingers M required for 50-Ω noise matching decreases. Thus, the DC power consumed from an LNA is expected to decrease as ω_o increases, as expected from Eqn. 2.30.

The optimum noise reactance (see Eqn. 2.31) is equivalent to the input device reactance. Both reactances are matched with a series gate inductor, whose ohmic losses contribute to the overall noise factor. When increasing the device width, the input matching inductor size shrinks along with its associated ohmic losses, thus the noise factor decreases, which imposes a trade-off between noise figure and power consumption.

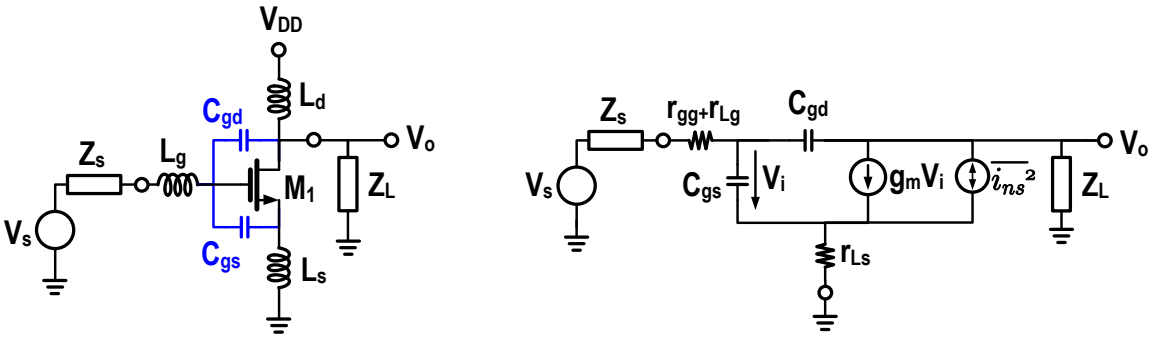
2.3.3 LNA Circuit Topologies

Fig. 2.17a shows one of the commonly used LNA circuit topology using inductive degeneration. The input impedance looking at the gate can be approximated by [56] :

$$Z_{eq}(s) \approx \frac{g_m L_s}{C_{gs}} + \frac{1}{sC_{gs}} + sL_s. \tag{2.32}$$

The real part of the input impedance is a function of L_s, so it can be used to adjust the input resistance to 50 Ω without changing the noise resistance. Moreover, the imaginary part includes L_s, so the gate inductor required for simultaneous noise and power matching is reduced to become :

$$L_g = \frac{1}{s^2 C_{gs}} - L_s. \tag{2.33}$$



(a) (b)

Figure 2.17: Low-noise common source amplifier: (a) circuit schematic and (b) small-signal noisy model

This topology has several drawbacks. Firstly, increasing inductor L_s reduces the amplifier gain, as it degenerates the source terminal. This is a problem at mm-wave frequencies, as the gain is inversely proportional to f^2 (see Eqn. 2.24). Secondly, if C_{gd} is not neglected in the analysis, the input return loss is reduced. Thirdly, the input Miller equivalent capacitance $[C_{dg}(1 + |A_v|)]$ limits the amplifier bandwidth. Moreover, C_{gd} creates a path for the device noise power from the output node to the input node as shown in Fig. 2.17b, thus degrading the overall noise performance of the amplifier.

Another amplifier circuit is the cascode configuration [56] shown in Fig. 2.18a. This configuration relaxes the common-source amplifier problems, which include insufficient gain, bandwidth limitation due to the Miller effect, and poor reverse isolation. The cascode amplifier consists of a common-source amplifier connected in series with a common-gate amplifier.

The cascode amplifier realizes higher gain compared to common-source configuration, as the output impedance increases. The Miller effect of C_{gd} of M_1 (see Fig. 2.18a) is relaxed due to the low input impedance seen at the source terminal of M_2, so the bandwidth is improved. Moreover, M_2 isolation enhances the reverse isolation of the amplifier.

Several drawbacks have been addressed in the cascode configuration. Firstly, the overall noise figure of the amplifier increases due to adding M_2, as part of the current noise power of M_2 has a signal path to Z_{o1} (see Fig. 2.18b). Secondly, the cascode amplifier linearity is degraded for a fixed V_{DD}, as the output voltage headroom is reduced. This is due to adding 2 devices in series between V_{DD} and ground. As a result, the supply voltage has to be increased to maintain the same linearity performance of the common-source amplifier, which results in larger power consumption.

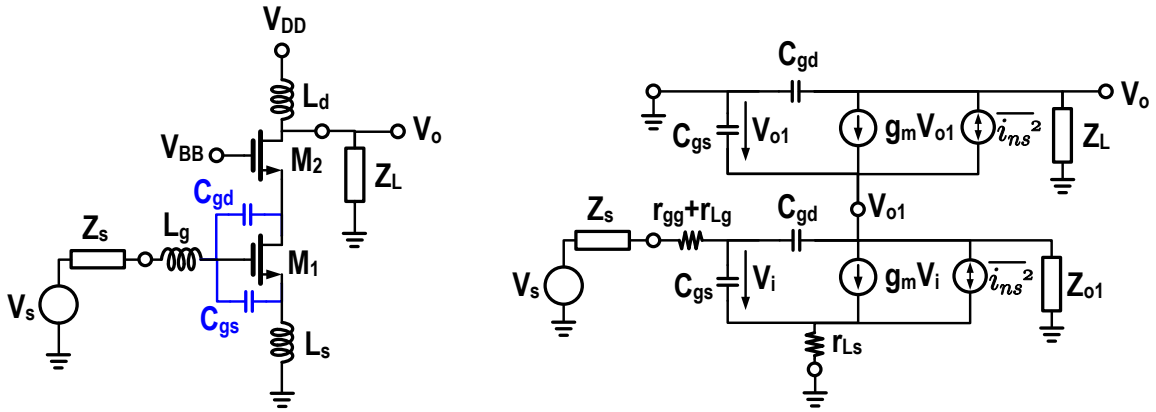


Figure 2.18: Low-noise cascode amplifier: (a) circuit schematic and (b) small-signal noisy model

Fig. 2.19a shows a transformer-feedback common-source LNA [57] between drain and source terminal. The circuit principle is based on performing feedback to the gate through H_{gs}, to counteract the intrinsic feedback due to H_{gd}. Assuming the transformer is ideal, and setting $H_{gs} = -H_{gd}$, the ratio between C_{gs} and C_{gd} can be approximated as follows :

$$\frac{C_{gs}}{C_{gd}} \approx n. \tag{2.34}$$

Since C_{gd} is neutralized by C_{gs}, the Miller effect is canceled. Gain and reverse isolation are improved. Moreover, the noise contribution through C_{gd} is suppressed. Additionally, the neutralization bandwidth depends on the turns ratio n of the transformer (i.e., wide bandwidth neutralization), however, it is determined by the transformer bandwidth in practice.

Another transformer-feedback configuration is shown in Fig. 2.19b, where the feedback is from the source inductor to the gate inductor [58]. The analysis in [58] shows that the input impedance can be approximated as :

$$Z_{in} \approx \frac{n^2}{(n+1)g_m}. \tag{2.35}$$

Wideband matching can be achieved at the input port, as n and g_m are both frequency-independent. One drawback, however, is that the overall noise figure increases due to

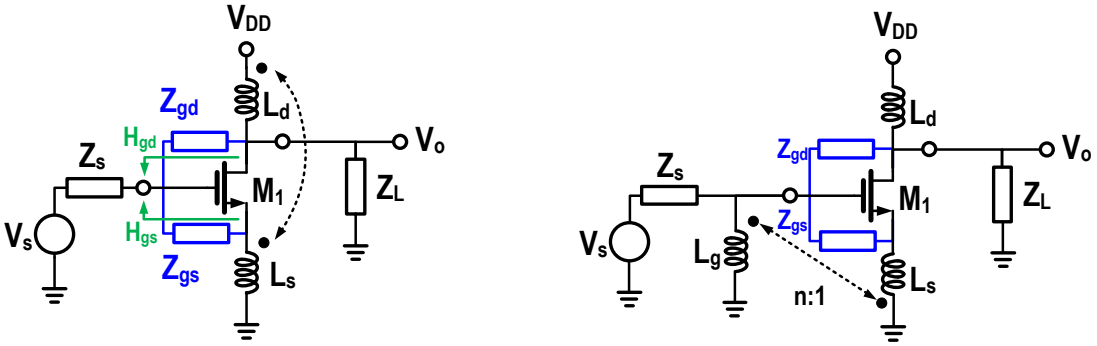


Figure 2.19: Transformer-feedback LNA configurations: (a) drain to source feedback and (b) source to gate feedback

the ohmic losses of L_g. Moreover, the interwound capacitance at mm-wave frequencies decreases f_t, as it adds up to the intrinsic C_{gs} of the amplifier.

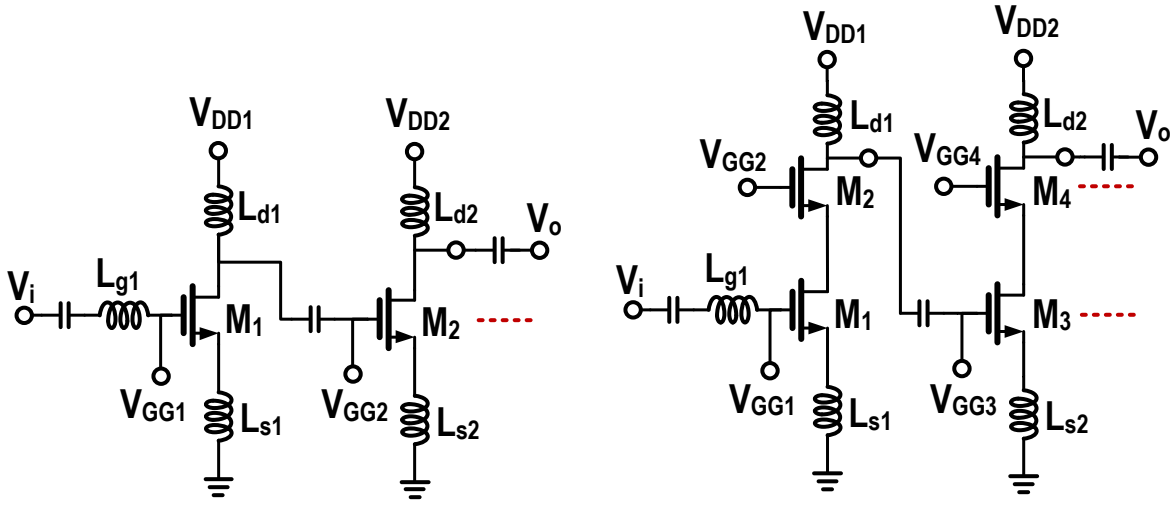
2.3.4 CMOS mm-Wave LNA Implementations

The amplifier's maximum available gain degrades, as frequency increases, so multistage amplification is required. Fig. 2.20 shows the most commonly used mm-wave LNA circuits in the literature [23, 59–63]. When a higher gain is required, more stages are cascaded. The design of passive components can be realized using lumped inductors (see Fig. 2.20), or distributed transmission lines (TL) [23]. However, TLs are avoided in this work, as they consume a larger physical area when compared to lumped inductors. All the transistors are biased at their optimum current densities $(\frac{I_{ds}}{W})_{opt}$ realizing NF_{min}.

inductors L_{s1} and L_{g1} (see Fig. 2.20) realize simultaneous noise and power matching to 50 Ω at the input port. L_{d2} tunes and matches the amplifier output to 50 Ω. L_{d1} and L_{s2} perform the interstage noise and power matching. Choosing the interstage matching impedance at 50 Ω [62] simplifies the design, when cascading more stages is needed.

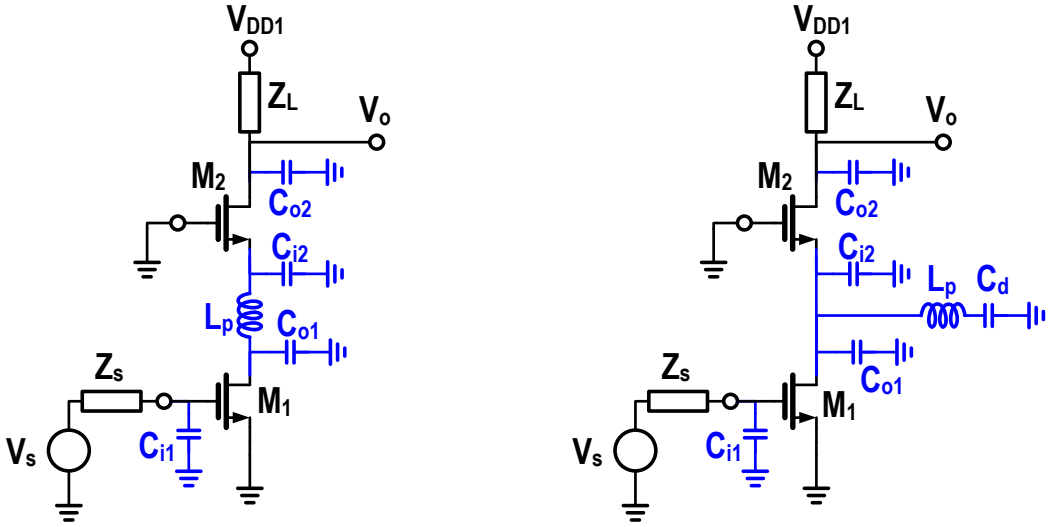
Another circuit topology is shown in Fig. 2.21 [64, 65] for bandwidth extension. The bandwidth of cascode amplifier is determined by the RC time constant of the equivalent tuned circuit, which can be given by :

$$\tau = R_s C_{i1} + R_{o1}(C_{o1} + C_{i2}) + R_L C_{o2}. \tag{2.36}$$



(a) (b)

Figure 2.20: mm-Wave multistage LNA circuit schematics: (a) cascaded common-source stages and (b) cascaded cascode stages



(a) (b)

Figure 2.21: Tuned cascode inductive peaking architectures with parasitic capacitance of different nodes highlighted (a) series peaking (b) shunt peaking

The intermediate node is the dominant pole of the cascode structure. Thus, by adding a series or shunt inductor at this node, the intermediate capacitance can be tuned and the bandwidth can be extended. A detailed analysis of L_p is found in [64,65]. Inductive peaking can be realized using lumped inductors, or coplanar waveguide (CPW) transmission lines, which occupy a large physical area.

A performance summary between different mm-wave LNA designs from recent literature is shown in Table 6.2. The selected designs are across different frequency bands, mostly in the 45-nm SOI-CMOS technology, where the proposed LNA is fabricated. As frequency increases on the same technology as in [23, 59, 62], the minimum NF increases, as expected from Eqn. 2.25. The power consumption decreases, as 50-Ω matching requires a smaller number of fingers as expected from Eqn. 2.30. Moreover, it is anticipated from the chip photos of [23] that the active area is larger than the other reported designs, as they incorporate CPW transmission line matching.

Table 2.3: Performance Summary of mm-Wave LNAs from Recent Literature

	[59]	[62]	[23]	[23]	[23]	[61]
Tech.	45nm-SOI CMOS	45nm-SOI CMOS	45nm-SOI CMOS	45nm-SOI CMOS	45nm-SOI CMOS	65nm CMOS
Topology	2-Stage Cascode	2-Stage CS/Cascode	2-Stage Cascode	2-Stage Cascode	3-Stage Common Source	3-Stage Common Source
Freq. (GHz) [S_{11}<-10dB]	42.5-55[1]	19-30[1]	43-57	58-80	84-88	63-67[1]
Gain (dB) [-3dB-BW(GHz)]	18.5 (43-53)[1]	19.5 (16-24)	15 (40-53)	12.5 (60-73)	13.5 (76-88)	23 (57-64)[1]
Noise Figure (dB)	2.9@47G	2@19G	3.3@45G	4@65G	5.7@85G	4
Output P_{1dB} (dBm)	3	0	1.5	-2	-1.5	-3.5
Supply Voltage (V)	1.2	1/1.5	1.3	1.3	1	1.25
DC Power (mW)	22.8	32.5	20.8	15	13.5	8
Active Area (mm^2)	0.14	0.15	—	—	—	0.05

[1]Estimated from the plots

Chapter 3

Phased-Array System Design

3.1 Introduction

As described in Chapter 1, increasing the frequency of operation enables wideband operation, while the physical area occupied by silicon chips required to support higher frequency bands increases for a phased-array implementation. Greater channel capacities (C) can be achieved at mm-wave bands when the channel bandwidth (B) increases, according to Shannon's theorem [66] :

$$C = B.log_2(1 + SNR). \quad (b/s) \tag{3.1}$$

However, these advantages come at the expense of larger path loss and therefore limited separation distances between the transmitter and the receiver in a radio link, as discussed in Chapter 1. The received power level for a radio link (see Fig. 3.1) may be predicted from Friis' formula [67] :

$$P_{R(dBm)} = P_{T(dBm)} + G_{T(dBi)} + G_{R(dBi)} - 10.log\left(\frac{(4\pi R)^2}{\lambda^2}\right), \tag{3.2}$$

where P and G are the transmitter or receiver power level and antenna gain, respectively.

Eqn. 3.2 predicts that as signal wavelength (λ) decreases (i.e., increasing carrier frequency), the received signal power decreases dramatically. As a result, the receiver signal-to-noise ratio (SNR) decreases and the bit-error-rate (BER) of the received information degrades. One possible solution is to increase the transmitter generated power, however,

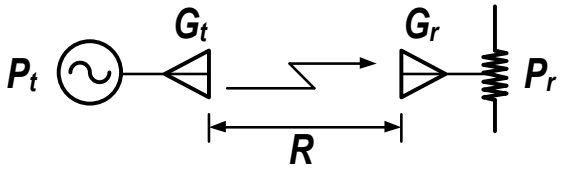
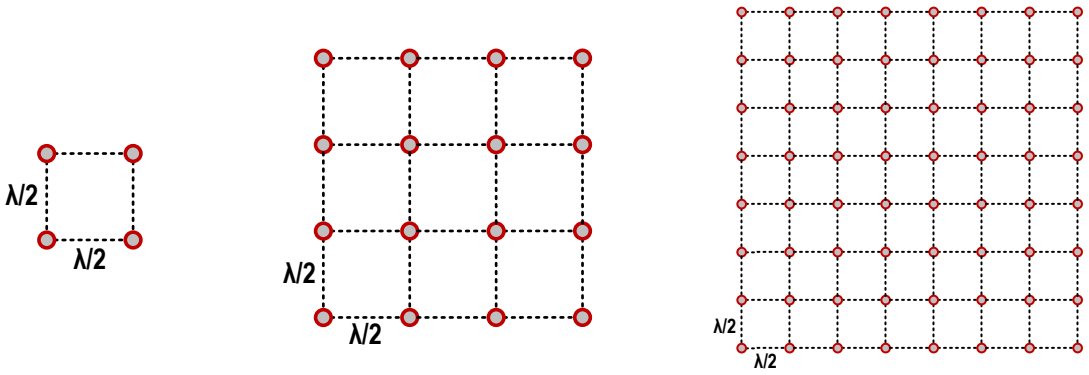


Figure 3.1: A simple radio transceiver system [54]



(a) (b) (c)

Figure 3.2: Different configurations of 2D linear antenna array spaced by $\lambda/2$ incorporating isotropic antennas: (a) 2×2, (b) 4×4, and (c) 8×8

the typical maximum output power available from a silicon CMOS power generation at 60 GHz is limited to less than 25 dBm [27]. Another solution is to use a phased-array antenna to increase the gain in the path between transmitter and receiver gain and thereby compensate for the increasing channel loss at higher frequencies.

3.2 Modular Phased-Array Transceiver Architectures

The operating principle of a phased-array receiver is illustrated in Fig. 3.3. The modulated signal is received over several paths. Each receive path consists of an RF antenna, a gain block, and an electronic phase shifter. The receive antennas form an array by placing them with an approximate separation distance of $(\lambda/2)$.

The antenna array creates an electrical signal that increases in signal amplitude when oriented in a specific direction and suppresses signal reception in any other direction. The direction where to received signal is maximized may be controlled by electronic phase

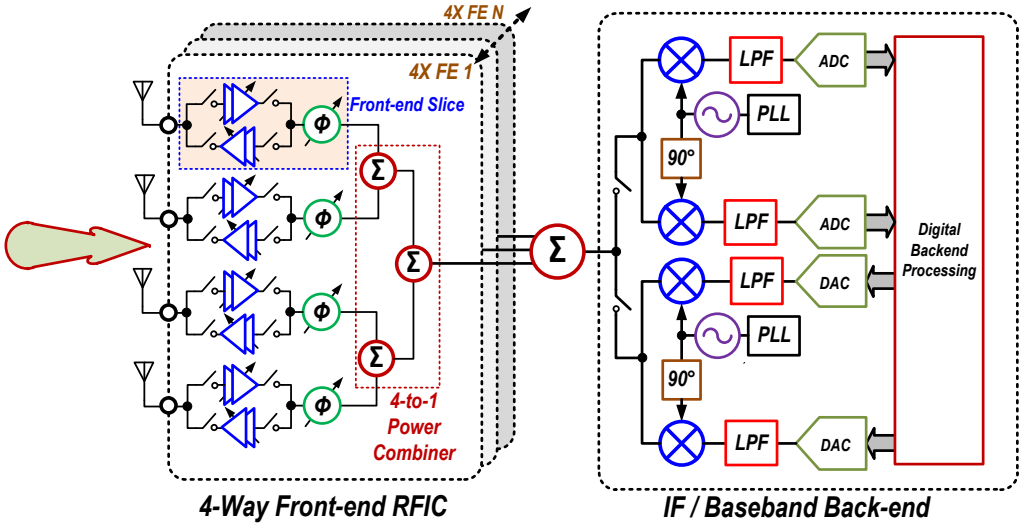
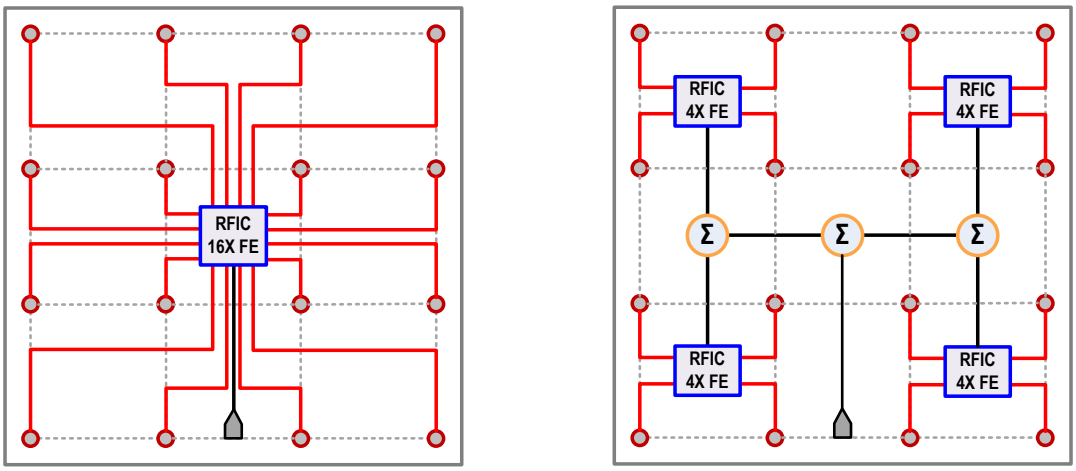


Figure 3.3: Phased-array transceiver system block diagram

shifters. When optimizing reception, a particular phase shift is assigned to each receive path according to the phase gradient corresponding to the receive direction. The desired signal is realized by combining the power received from each antenna in the array. The combined RF signal is then down-converted by a mixer to an intermediate frequency (IF) or baseband for detection, depending on the type of the receiver.

Off-chip packaging interconnects are lossy, especially at mm-wave frequencies. As a result, the packaging interface between the silicon chip and antenna modules has to be devised such that the interconnects are as short in length as possible. Fig. 3.4 shows two possible assembly scenarios for a case study of a 4×4 antenna array with RFIC front-end modules. Although the design spacing between 2 successive antennas (i.e., $\lambda/2$) decreases as the carrier frequency increases, the footprint of silicon chips is still smaller than the antenna array. Fig. 3.4a shows a 16× RFIC module interfaced with 4×4 antenna array module at the center. The red lines represent the off-chip interconnects, and the black line represents the power combined RF signal. It can be seen that the interconnect length varies with antenna coordinates in the array. Therefore, the RF signal experiences non-uniform loss and phase shift across each antenna, and become severely attenuated for the antenna connections at the 4 array corners. This can be seen from the interconnect length from the RFIC module to the antenna elements close to the 4 corners of the antenna module. This assembly floorplan deteriorates the performance, especially with array scaling.

Fig. 3.4b shows a more uniform distribution of the RFIC modules across the antenna



(a) (b)

Figure 3.4: Floor plan of RFIC and antenna packaging assembly (a) 4×4 array with 1 module of 16× RFIC front-end (b) 4×4 array with 4 modules of 4× RFIC front-end

array. A 4× RFIC module is positioned in the center of the 2D 2×2 antenna sub-array, where the interconnect length is short and uniform. RF signals from the different modules are then combined using on-chip transmission-lines and power combiners that can be relatively low-loss when designed on-chip. This assembly technique is more efficient and scalable across different array sizes.

3.3 45-nm SOI-CMOS Technology Fit

As discussed in Chapter 1, the 45-nm SOI technology node is a good candidate for mm-wave design because of the f_t and f_{max} performance possible when compared with older CMOS technology nodes. Also, the high integration density possible in CMOS technologies makes it a suitable choice for highly-integrated SoCs. However, a phased-array system has to also be assessed in terms of DC power consumption versus array size. A reasonable wireless handset peak effective isotropic radiated power (EIRP) of 30 dBm is assumed for this study, and the EIRP of an access point is assumed to be 50 dBm. Recent results from the literature show that CMOS power amplifiers are capable of delivering 20-dBm peak-P_{1-dB} with 26% peak power added efficiency (PAE) in SOI technologies [27]. The peak-to-average power ratio (PAPR) of the 802.11ad signal is close to 9 dB. Thus the transmitter average EIRP is set to 21 dBm (i.e., power back-off by 9 dB).

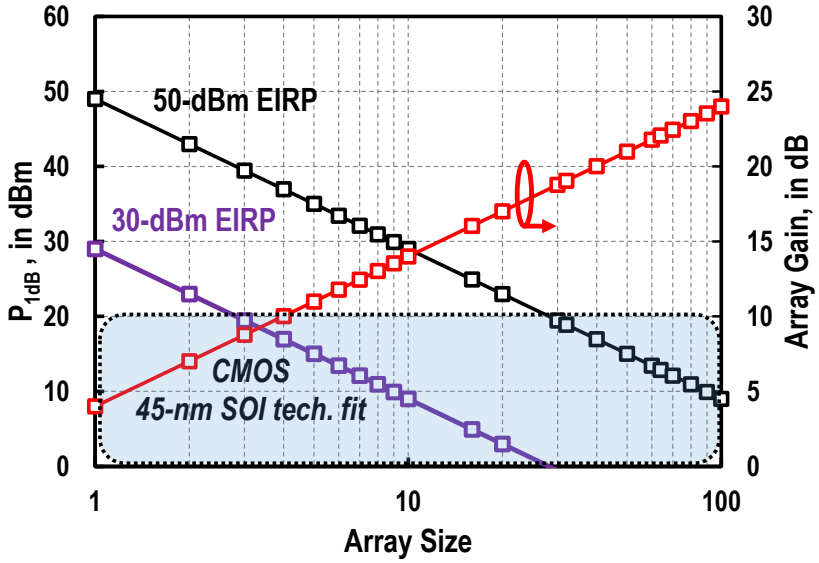
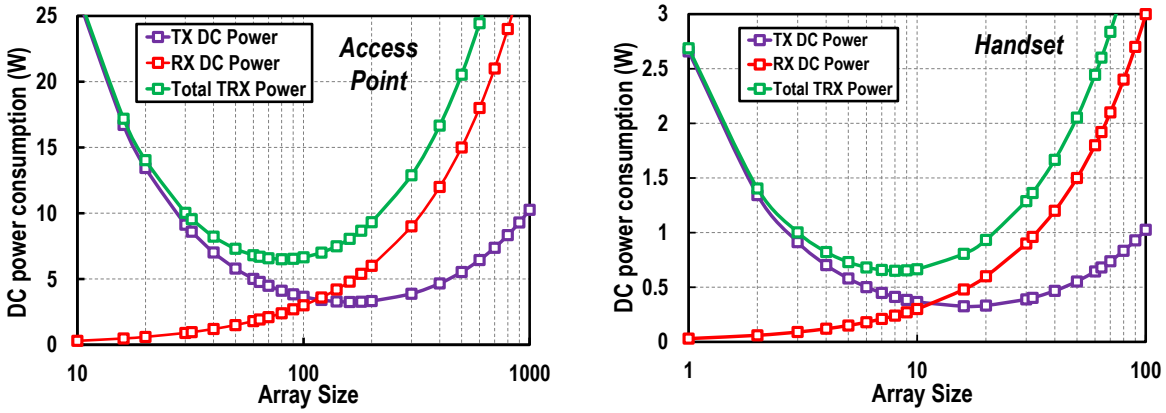


Figure 3.5: Single transmitter 1-dB compression point and array gain versus array size for 50-dBm and 30-dBm EIRPs



(a) (b)

Figure 3.6: Estimate for DC power consumption of a phased-array front-end transmitter, receiver and transceiver for (a) access point (b) handset

Figure 3.5 shows the 1-dB compression point and array gain for a transmitter slice versus array size for 50-dBm and 30-dBm EIRPs. Increasing the order of the phased array relaxes the transmitter power limits, and hence the DC power consumption. Figure 3.6

estimates the total DC power consumption of both phased-array transmitter and receiver assuming a constant receiver DC power consumption of 30 mW per element. For a small array size (i.e., 2 to 4), the power consumption is limited by the transmitter, whereas for a large array-order (i.e., beyond 100) the receiver dominates the total power consumed. From Fig. 3.6a, an array order of 64 for an access point is optimum to achieve a minimum DC power of approximately 6.8 W for the same peak EIRP of 50 dBm. This DC power may be consumed from a fixed point power supply. On the other hand, an array order of 16 requires a DC power consumption of around 0.8 W, as shown in Fig. 3.6b. It should be noted that the array size may be adjusted according to the interconnect power losses between transceiver blocks to achieve the target EIRP. Alternatively, the transmitter RF power may be increased to account for the stated losses.

3.4 Link Budget Case Study

Transceiver specifications depend on the target up-link (UL)/down-link (DL) data rates, as well as the modulation schemes supporting those rates. Therefore, the design is application dependent. Additionally, mm-wave network deployment is subject to the surrounding environment and whether the communication link is in direct line-of-sight (LOS) or non-line-of-sight (NLOS) [11].

Figure 3.7 describes different factors affecting the link budget calculations and receiver sensitivity. To receive the transmitted signal properly, the receiver must satisfy a minimum signal-to-noise ratio (SNR). The lower bound of the SNR is the thermal noise floor, which is determined by the signal bandwidth, the receiver noise figure (NF), and the array antenna gain. As a result, the front-end switches and low-noise amplifiers have to be carefully designed for minimal noise contribution. On the other hand, the upper bound of the SNR is determined by the receiver linearity to prevent signal compression.

As a starting point, the upper bound of the downlink (DL, 64-QAM) of 6.75 Gbps and that of the uplink (UL, 16-QAM) of 4.5 Gbps is assumed. The minimum corresponding signal-to-noise ratios (SNR) for proper signal detection are 27 dB for the UL and 21 dB for the DL, respectively, assuming a bit-error-rate (BER) of 10^{-6}. The maximum channel width is 0.75 GHz for UL and 0.64 GHz for DL (i.e., Claude Shannon prediction from Eqn. 3.1).

Table 3.1a shows transmitter assumptions for both UL and DL. From minimum power consumption considerations, the handset array size is set at 16, and that of the access point is set to 64. An antenna element gain of 7 dBi [68] and front-end switch losses of 3 dB are

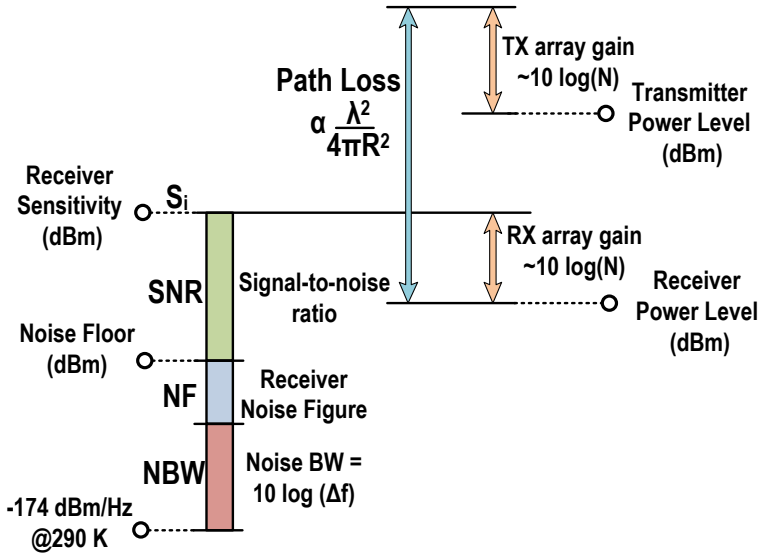


Figure 3.7: Phased-array link budget parameters

assumed. Table 3.1b displays transmitter specifications for both UL and DL assuming 135-dB T-R path power loss for both links. Finally, Table 3.2 presents the receiver sensitivity analysis for both UL and DL based on the assumptions of Table 3.1a. A receiver NF of 6 dB is assumed. It includes front-end switch losses and the input-referred NF of the front-end receiver chain.

From Table 3.2, a minimum handset receiver gain (per front-end slice) of 8 dB is required to maintain the minimum 21-dB SNR of the 16-QAM signal at 4.5 Gbps. An access point receiver gain per slice of 16 dB is required to maintain the same SNR. Another receiver sensitivity analysis of 2 access points is also shown in Table 3.2. The analysis predicts a received SNR of 41 dB, which supports both 16-QAM and 64-QAM (i.e., 6.75 Gbps) signals assuming that the receiver per-slice gain is set to 16 dB. As a result, access point separation can support a larger distance as long as the receiver SNR is maintained well above 27 dB. A single-slice receiver gain of 8 dB is deduced from the study. This doesn't include the 3 dB switch losses. Therefore, the gain of the cascaded SPDT switch, low-noise amplifier, SPDT switch, and phase shifter has to be maintained above 8 dB. Based on the literature survey and selected technology simulations, a 3 dB insertion loss (IL) is assumed for the SPDT switch, a 6-dB IL is assumed for the passive phase shifter and a 20 dB gain is assumed for the low-noise amplifier. This case study assumes 3-dB power combining losses at both transmitter and receiver.

Table 3.1: Up-link/Down-link Transmitter Assumptions and Specifications for 60-GHz channel of 100-m T-R Separation

(a) Transmitter Assumptions

Assumptions	Access Point	Handset
P_{1dB}/PA(dBm)	13	5
No. of PAs	64	16
No. of ANT	64	16
ANT Gain(dBi)	7	7
SW Loss(dB)	3	3

(b) Transmitter Specifications

Specifications	Access Point	Handset
Tx Power(dBm)	31	17
Tx ANT Gain(dB)	25	19
Tx Peak EIRP(dBm)	53	33
Tx Avg. EIRP(dBm)	44	24
Path Loss(dB)	135	135

Table 3.2: Up-link and Down-link Receiver Sensitivity Analysis

60-GHz Link Budget for 100m T-R Separation	Handset	Access Point	Access Point 2
Receiver Power (dBm)	-91	-114	-94
Thermal Noise Floor (dBm)	-86	-86	-85
Rx Noise Figure (dB)	6	6	6
Rx Antenna Gain (dB)	19	25	25
Number of Rx Slices	16	64	64
Rx Slice Gain (dB)	8	16	16
Rx Power after Beamforming(dBm)	-55	-55	-35
Rx SNR after Beamforming(dB) (3-dB Combining Losses)	22	22	41

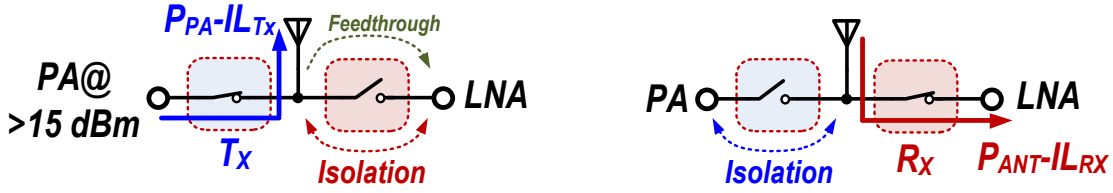
Chapter 4

CMOS SPST/SPDT Front-End Switch Designs

4.1 Introduction

A wideband transmit-receive (T/R) RF switch occupying minimal chip area in CMOS is an essential element in half-duplex phased-array or reconfigurable radio front-ends. Fig. 4.1 illustrates transmit and receive modes implemented using single-pole, single-throw (SPST) switches at the antenna. Isolation between the transmit power amplifier (PA) and the low-noise amplifier (LNA) is provided by a switch.

The performance of conventional series-shunt SPST topologies in CMOS is limited by area constraints on the switch transistors at RF and mm-wave frequencies. For example, if the transistor area is increased to lower insertion loss (IL) in the ON state, the port-to-port isolation (ISO) when the switch is turned OFF degrades due to parasitic coupling between



(a) Transmit (b) Receive

Figure 4.1: mm-Wave Tx/Rx front-end incorporating SPST switches

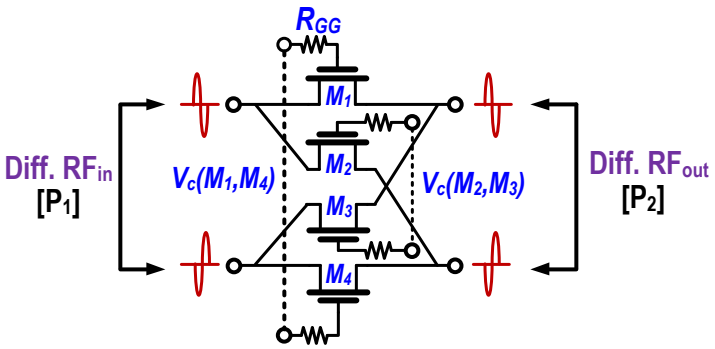


Figure 4.2: Simplified schematic of the proposed SPST switch

ports (i.e., IL vs. ISO trade-off with the area). Other designs, such as transmission-line-based switches [37–39], occupy more chip area and are inherently narrowband. The fully-differential, wideband SPST switch proposed in this work realizes better than 50-dB isolation through the cancellation of parasitic coupling at RF between terminals in the OFF state. Since higher port-to-port isolation is possible with the new circuit topology, larger-area switch transistors are used to reduce insertion losses.

Objectives for the wideband SPST switch developed in this work are: 1) greater than 50-dB isolation between RF ports in the OFF state, and less than 3-dB insertion loss in the ON state, 2) linearity consistent with the maximum PA outputs available on-chip in CMOS (e.g., greater than +15 dBm compression), and 3) bandwidth sufficient for mm-wave applications below 44 GHz.

4.2 High-Isolation SPST Switch Design

In this work, the cancellation of substrate RF parasitic coupling is used to realize greater switch isolation (ISO). The fully-differential switch realizes a much larger ISO than previous designs, and it is relatively insensitive to transistor sizing. From a simplified switch analysis presented in the following sub-section, it will be shown that insertion loss (IL), while insensitive to the switch on-resistance R_{ON}, is dictated by the device time constant $R_{ON}C_{OFF}$. This time constant also determines the upper-frequency limit for switch operation, f_o. The frequency response ranges from f_o down to DC. Furthermore, a new biasing scheme is proposed to increase the RF power compression of the switch beyond that realized using conventional biasing methods.

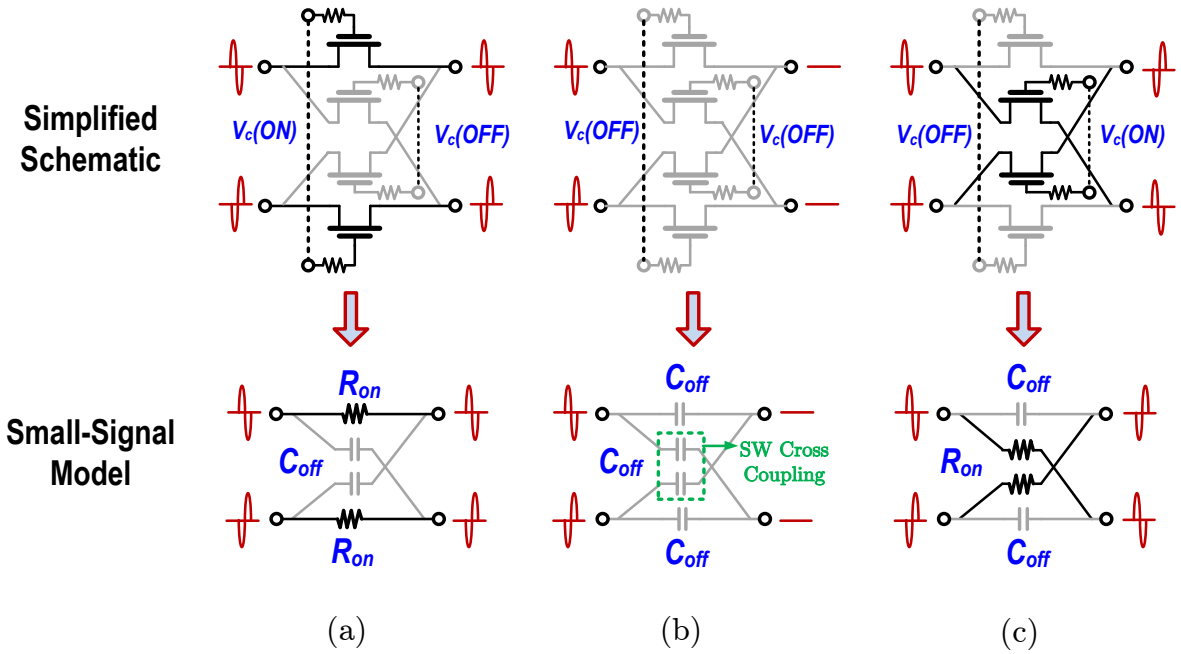
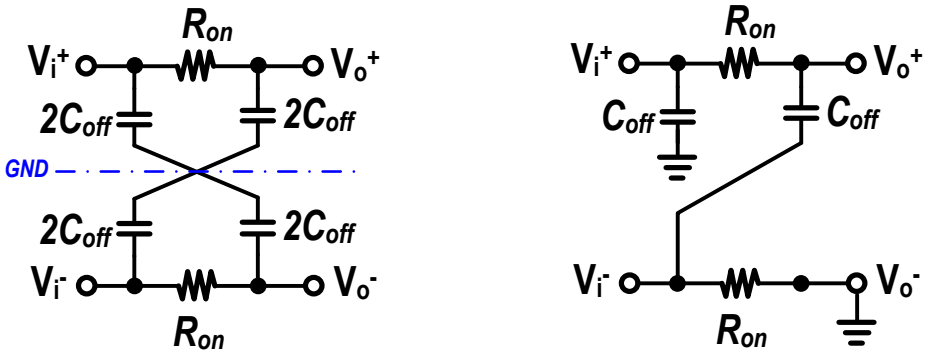


Figure 4.3: Simplified SPST schematics and small-signal models for: (a) ON state (thru switches ON), (b) OFF state (all switches OFF), and (c) 180° phase shift state (cross switches ON)

4.2.1 Suppression of Parasitic RF Coupling

A simplified schematic of the switch developed in this work is shown in Fig. 4.2. The switch is intended for use in the fully-differential RF signal path of a mm-wave transceiver front-end. High isolation between the input and output in the switch OFF state is realized through compensation of parasitic RF signal coupling. To achieve this, an anti-phase RF signal (via M_2, M_3 in Fig. 4.2) is added to the parasitic signal coupled across switches M_1 and M_4. The compensation is designed to cancel any unwanted feedthrough. This cancellation is bilateral and is therefore effective when RF is applied at either side of the switch. Compensation is realized by a transistor (i.e., not a physical capacitor), which tracks the switch parasitics for changes in process, voltage, and temperature (i.e., PVT) variations for a more robust design.

Figs. 4.3a to 4.3c illustrate operating modes for the SPST switch. In the ON state, the main switches (dark lines) are biased ON, while cross switches (shaded) are turned OFF. The RF input signal passes from input to output, and vice versa in the ON state, since the



(a) (b)

Figure 4.4: Small-signal RC model of ON state switch: (a) half-circuit equivalent circuit (b) applying superposition by grounding V_o^-

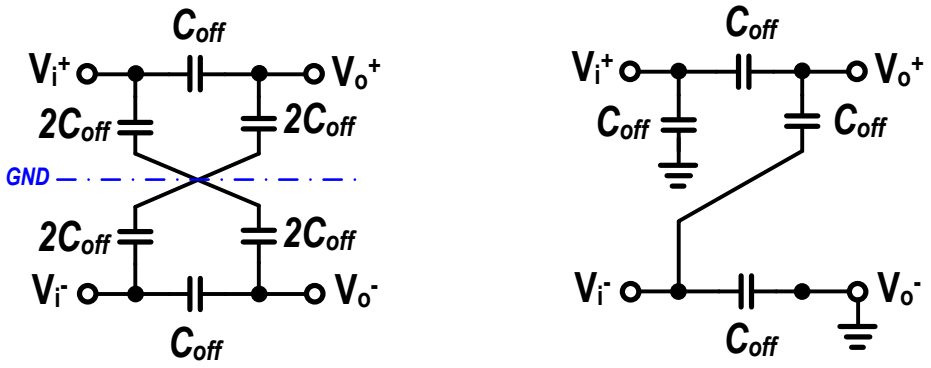
switch is bilateral. However, the parasitic capacitance of the switches (C_{OFF} in Fig. 4.3a) causes unwanted feedthrough of RF between the input and output in the OFF state that degrades isolation. When all devices are biased OFF (as in Fig. 4.3b), the anti-phase RF signal coupled via the compensation transistors cancels the in-phase RF feedthrough at each port when the coupling is made equal across all four paths, which improves isolation dramatically. Another advantage of this configuration is that the RF signal may be phase-shifted 180° by configuring the states of the main and cross transistors as shown in Fig. 4.3c.

4.2.2 Small-Signal Circuit Analysis

Fig. 4.4a shows the RC equivalent circuit of the ON state switch. Several assumptions are made in the following analysis. Firstly, $V_i^+ = -V_i^- = V_i/2$, and therefore the half-circuit principle can be applied to divide the circuit horizontally into two identical sub-circuits. Secondly, by superposition, V_o^- can be grounded so that V_o^+ is derived in terms of V_i^+ and V_i^- as shown in Fig. 4.4b. As a result, V_o^- is then deduced by swapping V_i^+ with V_i^-. Also, from superposition, V_o^+ in terms of V_i^+ and V_i^- may then be written as:

$$V_o^+ = \frac{1}{1 + sR_{on}C_{off}} V_i^+ + \frac{sR_{on}C_{off}}{1 + sR_{on}C_{off}} V_i^-, \tag{4.1}$$

where R_{on} is the equivalent ON resistance of the in-phase switches, C_{off} is the lumped-



(a) (b)

Figure 4.5: Small-signal C model of OFF state switch: (a) half-circuit equivalent circuit (b) applying superposition by grounding V_o^-

equivalent capacitance of the anti-phase switches in the OFF state, and s is the Laplace variable (i.e., $s = j\omega$ in the sinusoidal steady-state).

This equation can be further simplified, assuming V_i^- equals $-V_i^+$:

$$V_o^+ = \frac{1 - sR_{on}C_{off}}{1 + sR_{on}C_{off}} V_i^+. \tag{4.2}$$

Expressing the half-circuit transfer function in differential form yields:

$$V_o = \frac{1 - sR_{on}C_{off}}{1 + sR_{on}C_{off}} V_i. \tag{4.3}$$

Eqn. 4.3 predicts that IL at RF is determined by the time constant $R_{on}C_{off}$ of the CMOS switch. Its value is insensitive to transistor width but varies across technology nodes. Since the input impedance of the switch is capacitive, a series inductor is required at each port for 50-Ω matching. The total IL is expected to increase because of ohmic losses added by series matching inductors.

Fig. 4.5a shows the lumped-capacitance equivalent circuit of the OFF state switch. The same assumptions made for the ON-state switch are also applied to the analysis of the OFF-state switch. Again, V_o^+ is deduced using superposition by grounding V_o^- as shown in Fig. 4.5b. Provided that the in-phase and anti-phase switches have the same transistor

sizing, C_{off} seen by the 4 devices should be equal. As a result, V_o^+ (from superposition) is expressed as :

$$V_o^+ = \frac{V_i^+}{2} + \frac{V_i^-}{2}. \tag{4.4}$$

Assuming differential excitation where V_i^- equals $-V_i^+$, V_o^+ can be simplified to:

$$V_o^+ = V_o^- = V_o = 0. \tag{4.5}$$

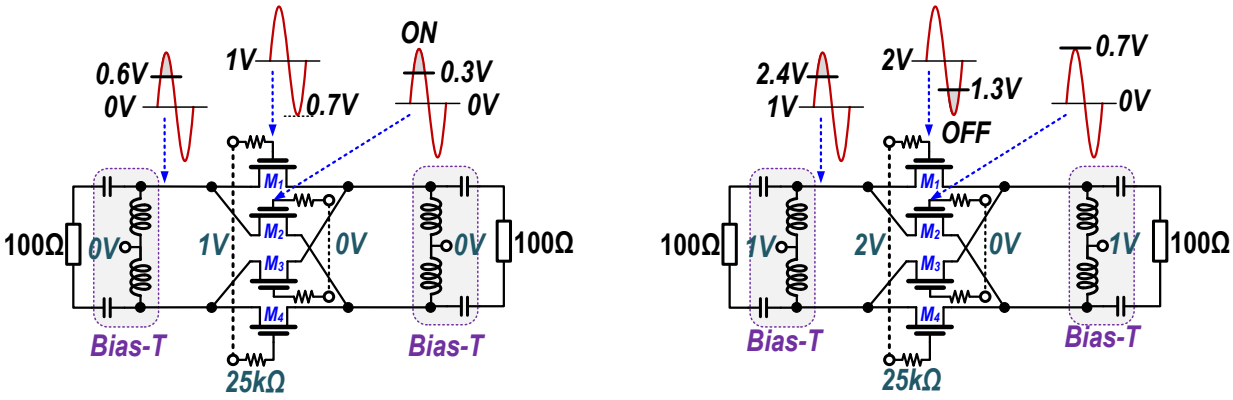
As a result, parasitic RF coupling is canceled completely at the output port of the simplified switch equivalent, thereby realizing port isolation greater than 50 dB in practice. Due to approximations made in this simplified analysis and sources of circuit mismatch, isolation degrades but is still higher than realizable with other (i.e., uncompensated) CMOS RF switch topologies.

4.2.3 Large-Signal Circuit Analysis

Large-signal switch performance is determined by the power handling capabilities of the transistors and the capability to connect multiple RF switches in series (e.g., transistor stacking) [21]. Floating-body devices available in SOI technologies offer improved power handling compared to bulk CMOS technologies, because the substrate parasitic diodes are always turned OFF and power leakage via the substrate is negligible. In this work, in addition to adopting floating-body devices, a new biasing scheme is proposed to further improve the RF power handling of the differential switch.

Fig. 4.6a shows a conventional biasing scheme applied to the proposed switch. The source and drain terminals of all devices are biased at 0 V. In the ON state, device M_1 is biased ON, while M_2 is biased OFF. As a result, M_2 is turned ON under a large signal RF input signal swing of 0.6 V-pk (V_{TH}=0.3 V assumed). Device M_1 is not experiencing compression, as the RF voltage minimum value of 0.7 V at the gate terminal is not low enough to turn it OFF.

Fig. 4.6b shows an improved biasing scheme for the proposed SPST switch. The V_{GS} is set at the maximum possible DC value (limited by oxide breakdown), which for the 45-nm SOI-CMOS technology used in this work is 1 V. RF signal lines are also biased to 1 V, while the gate bias shifts from 0 V in the OFF state to 2 V in the ON state. In the ON state, the transistor switch M_1 is ON, while M_2 is biased OFF. In this case, device M_1



(a) (b)

Figure 4.6: Large-signal switch performance and biasing (a) conventional (b) proposed

experiences early compression when the large-signal RF input voltage reaches 1.4 V-pk, or 0.8 V greater than the 0.6 V-pk RF signal input level attainable with conventional biasing of the switch. The gate terminal voltage reaches 1.3 V which turns M_1 OFF. Device M_2 is still turned OFF as the gate RF signal peak is set to 0.7 V, while the turn-ON voltage is 1.3 V. Based on the new biasing scheme, the power compression is pushed to an equivalent RF peak of 1.4 V instead of 0.6 V when the switch is biased conventionally.

4.2.4 Switch Design

A procedure for the design of the SPST switch, including transistor sizing and layout, is presented in this sub-section. A complete schematic of the fabricated prototype is shown in Fig. 4.7. Each switch unit (i.e., U_1 to U_4) is comprised of two CMOS transmission gates in series (i.e., M_1 and M_2 in Fig. 4.7), which increases the large-signal compression limit from 13 dBm to 20 dBm at the expense of increasing the IL from 0.7 dB to 1.4 dB at 30 GHz. The DC bias at the RF ports is set at 1 V, which is the maximum V_{GS} allowed in the 45-nm technology. The 115-pH inductance L_{feed} is used to match the input capacitance of the in- and anti-phase switches to a 50-Ohm source. The switch unit sizes are swept in simulation to optimize broadband operation, and an aspect ratio (W/L) of 20 μm/40 nm is selected for both NMOS and PMOS devices.

The gate control voltages are 0V for V_{CNM} and 2V for V_{CPM} in the ON state, and 2V V_{CNM} and 0V for V_{CPM} in the OFF state. Large-signal compression behavior is determined by the magnitudes of these bias voltages, and choosing maximum values improves

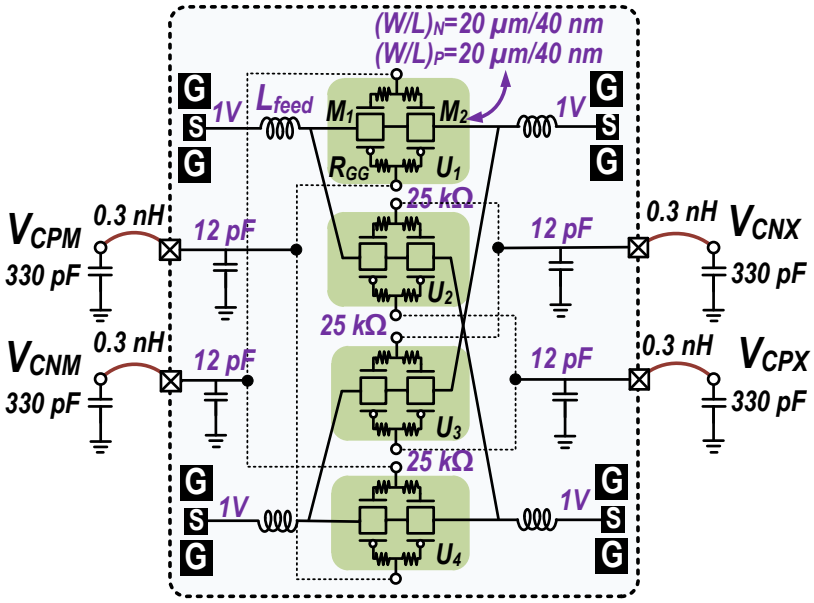


Figure 4.7: Schematic of the differential SPST switch prototype

the power compression and intermodulation distortion limits of the SPST switch. Isolation is optimized by keeping the SPST switch implementation (including physical layout) symmetric (e.g., differential feed lines are the same length).

4.2.5 Small-Signal Simulations

The small-signal S-parameters simulated for the differential mode (excluding the effects of metal fill) are plotted in Fig. 4.8. The input and output ports are broadband matched to 100 Ω, and the simulated return loss (RL) is greater than 10 dB across DC-50 GHz for the ON state condition. Simulated IL is less than 2.66 dB with a minimum of 1.4 dB at 1 GHz. The increasing trend in IL across frequency agrees with the response predicted by Eqn. 4.3. The OFF state isolation is better than 68 dB across DC-50 GHz. OFF state analysis from Eqn. 4.5 predicts infinite isolation. However, simulated isolation is finite due to implementation asymmetries and their parasitics.

CMOS processing variations are simulated using the Monte Carlo (MC) technique, where the simulator assigns global random parameters for each transistor instance in the design according to fabrication limits. The small-signal simulation results for 500 MC trials at 30 GHz are shown in Fig. 4.9. The predicted isolation is 72.7 dB (mean) with a variance

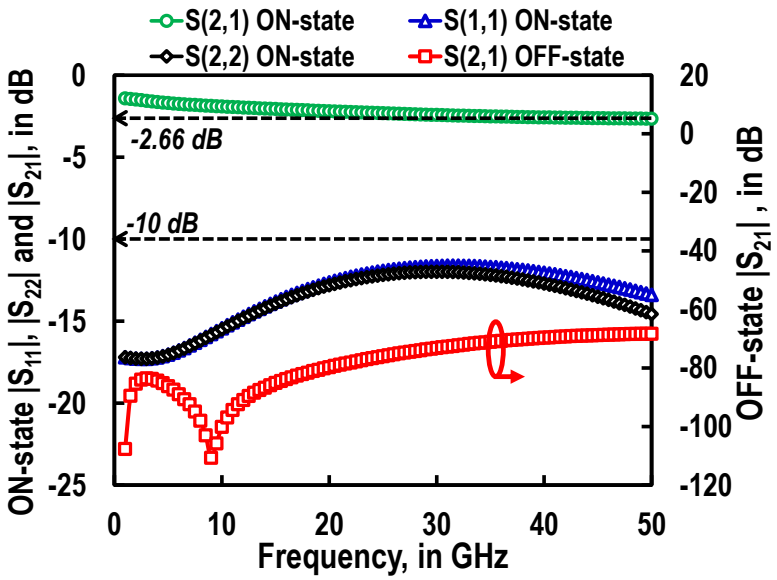


Figure 4.8: Simulated small-signal S-parameters (differential) in ON and OFF states

of ±2 dB and a standard deviation of 0.59 dB, as shown in Fig. 4.9a and Fig. 4.9b. The mean insertion loss is 2.41 dB with a variance of ±0.2 dB and standard deviation of 0.054 dB, as shown in Fig. 4.9c and Fig. 4.9d. Simulations predict a 2.75% maximum error in ISO and 8.3% maximum error in IL, which reflects the switchs robustness to process variations.

Supply variations are simulated by varying the voltage by ±5% (i.e., 1.9-V to 2.1-V supply). The resulting change in small-signal insertion loss at 30 GHz shows relatively little sensitivity, at just ±0.2 dB. Temperatures ranging from 0°C to 85°C are also investigated using simulation. The insertion loss and isolation vary by ±0.1 dB from their corresponding nominal values at 30 GHz.

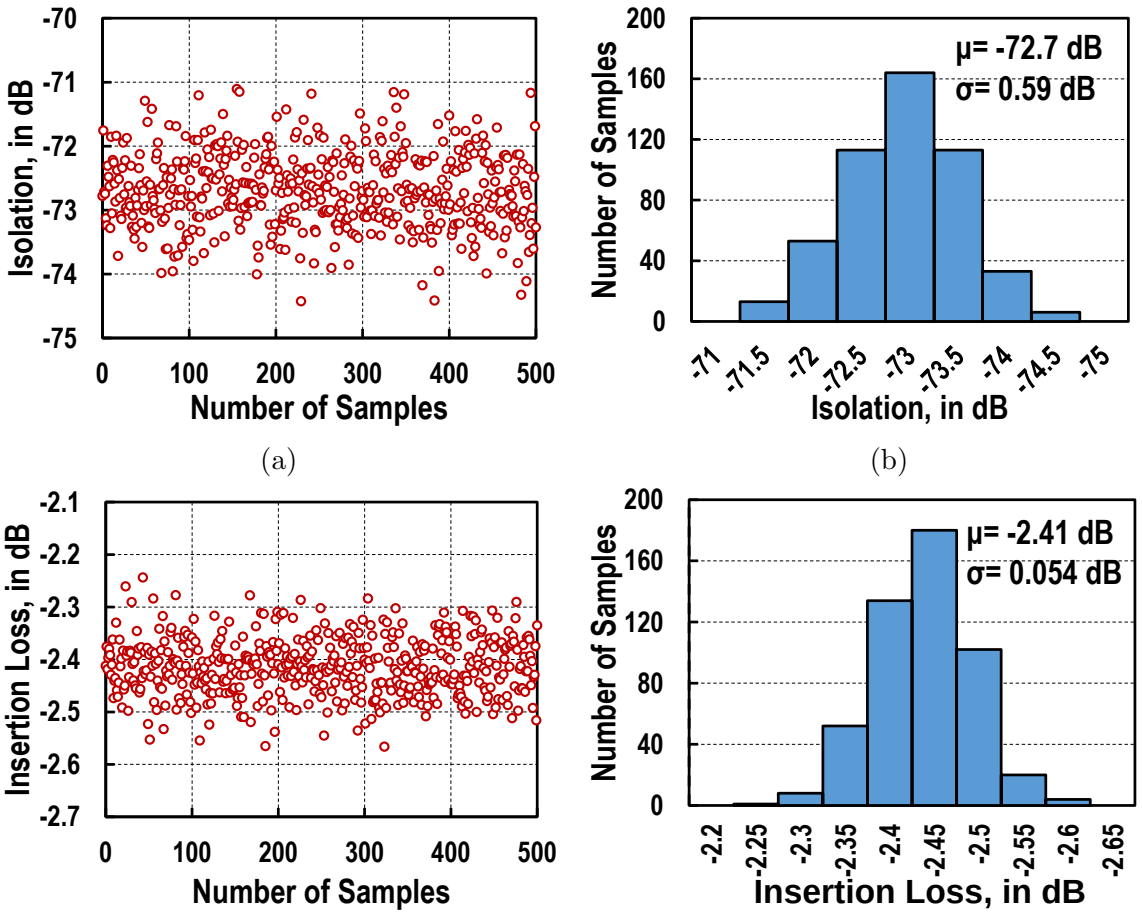


Figure 4.9: Monte Carlo simulation results at 30 GHz: (a) isolation data from 500 trials, (b) isolation mean and standard deviation, (c) insertion loss data from 500 trials, and (d) insertion loss mean and standard deviation

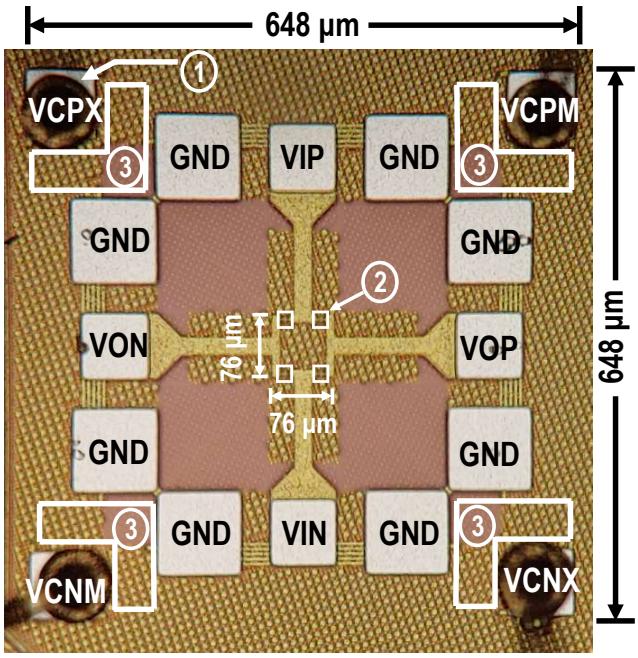


Figure 4.10: Micrograph of the fabricated prototype, with: (1) DC bias wirebond pads, (2) switch units and biasing resistors, and (3) 12-pF on-chip decoupling caps highlighted

4.3 Simulations vs. Measurements

A die photo of the fabricated prototype is shown in Fig. 4.10. The RF probe pad and top-metal feedline are designed to match each port to a 50-Ω source. RF losses of the feedlines are minimized by implementing them in 2.2-μm thick top metal from the 11-metal BEOL stack (Option 8) in GlobalFoundries 45-nm RF-SOI CMOS technology. The total active area for the switch is 0.0058 mm^2.

4.3.1 Small-Signal Measurements

The switch is characterized using an N5245B 4-port vector network analyzer (VNA). All small-signal parameters, including ON-state insertion and return loss (IL and RL, respectively), and OFF-state isolation (ISO) are measured on-die via RF probes with the set-up shown in Fig. 4.11. Differential measurements are realized by pairing ports of the VNA and exciting each port pair using the differential true mode stimulus option [69]. This enables phase sweeping of the signal at one port with respect to the other in a port pair.

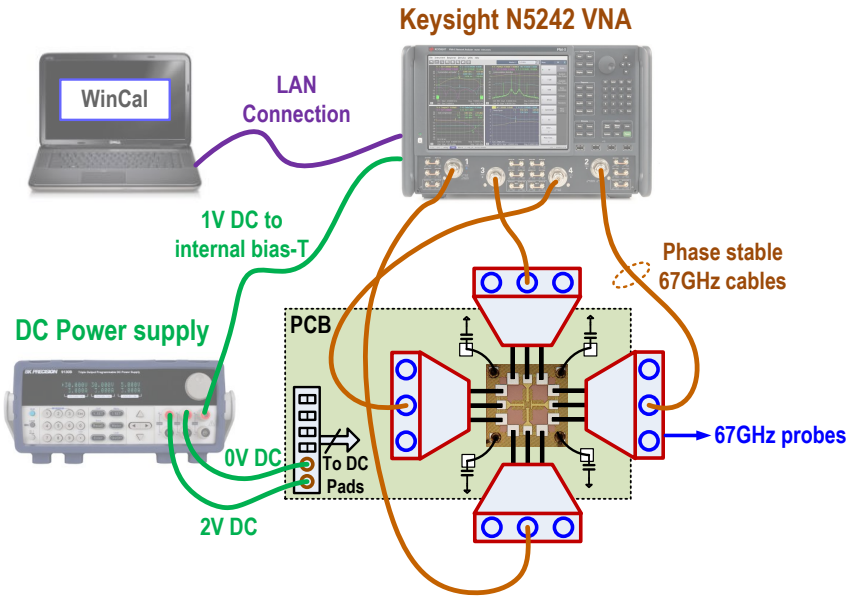


Figure 4.11: Experimental set-up for small-signal measurements

Parasitics and losses of the probe pads and 200-μm long feedlines are de-embedded from the small-signal data [70]. RF probes and VNA cables are calibrated with a standard substrate using WinCal software. A separate open-circuit test structure is measured to capture parasitics in shunt with each pad for de-embedding. A transmission line model for the feedlines is also used to de-embed losses from each line across frequency, including coupling to the substrate.

Isolation measured in the OFF state is plotted in Fig. 4.12. It exceeds 50 dB from DC to 43 GHz when the switch is driven differentially. The advantages of the proposed design are clear when single-ended isolation is compared to the isolation realized across differential port pairs. The single-ended isolation is just 12 dB at 40 GHz because there is strong parasitic RF coupling between the drain and source transistor terminals, mainly via the substrate. This RF coupling is effectively canceled when the proposed switch topology is excited differentially, and the measured isolation increases by more than 40 dB at 40 GHz.

The effect of differential phase error on isolation in the OFF state was measured at 4 frequencies. The results are plotted in Fig. 4.13. Ideally, the input is purely differential, with identical amplitudes and 180° phase difference (i.e., zero phase error). The through and cross-coupled paths of the switch are matched very well at 10 GHz, where 0° phase

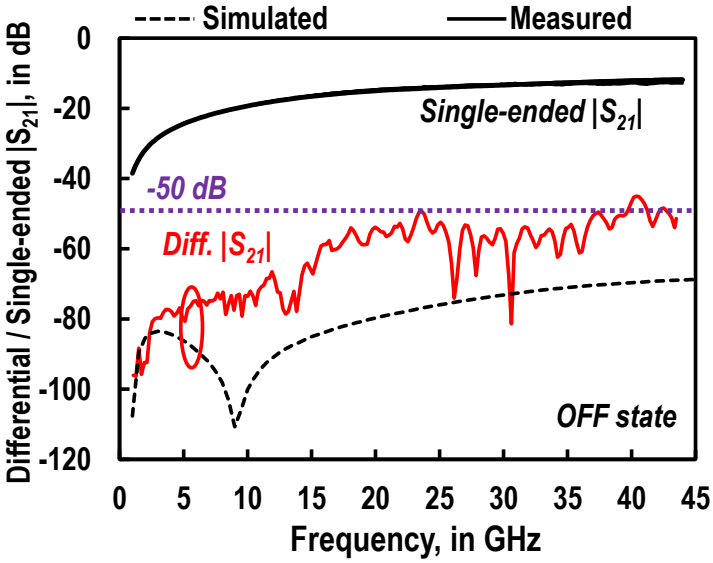


Figure 4.12: Measured isolation in the OFF state

error maximizes isolation. However, frequency-dependent mismatch, which is affected by parasitic capacitance mismatch between switching transistors, causes the phase error for maximum isolation to vary by up to ±20° as the input frequency rises. Nevertheless, isolation greater than 50 dB is attained across a wide range of phase error at 40 GHz, as seen from Fig. 4.13. The differential IL increases by 0.5 dB from its zero-phase-error value up to ±60° differential phase error. As a result, phase calibration has minimal impact on IL compared to isolation.

Small-signal measurements in the ON state for the SPST switch are shown in Fig. 4.14. Return loss (i.e., RL=$|S_{11}|$) exceeds 10 dB across the range from DC to 43.5 GHz. Insertion loss is less than 3 dB across the same band in both phase-shift states (i.e., 0° and 180°). The measured noise figure is consistent with the IL data (i.e., identical). Phase shift measured across frequency for the two-phase states is very close to the ideal (180°) as seen from Fig. 4.15. Relative phase shift measurements realize a maximum phase shift error of less than 1.4° across the entire band. The average group delay measured across frequency is flat at approximately 400 ps, as shown in Fig. 4.15.

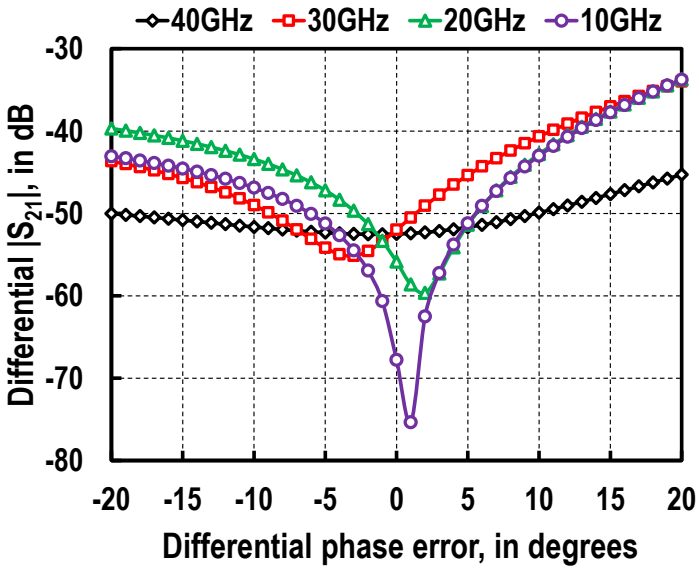


Figure 4.13: Measured isolation in the OFF state vs. differential phase error

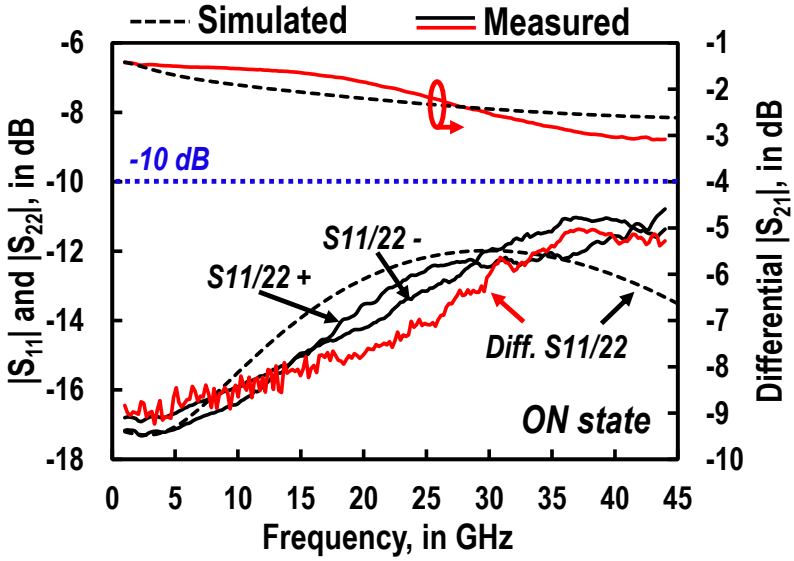
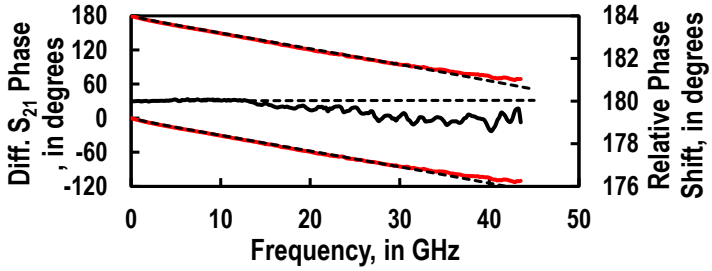
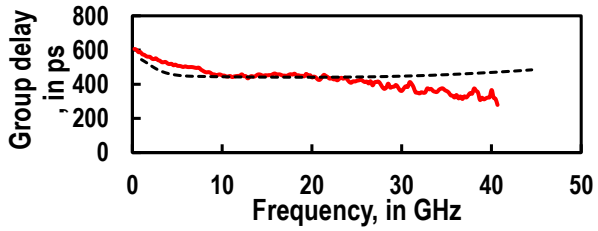


Figure 4.14: Measured and simulated $|S_{11}|$ and $|S_{21}|$ vs. frequency for the SPST switch in the ON state



(a)



(b)

Figure 4.15: SPST switch phase response: (a) phase shift states and relative phase shift vs. frequency (b) group delay vs. frequency. Measured data plotted as solid lines and simulation results as dashed lines

4.3.2 Large-Signal Measurements

An external wideband amplifier (DC-24 GHz with P_{1dB}=27-dBm max.) is used to attain the power levels required to characterize large-signal compression and intermodulation behaviors of the switch (see the experimental set-up of Fig. 4.16). Compression of IL in the ON state is independent of the excitation mode (i.e., differential or single-ended), therefore single-ended excitation is used to avoid balun losses at the switch ports used for single-ended-to-differential conversion. Since the RF port bias is blocked by the PA, a broadband bias-T is used to bias the input port to 1 V, as shown in Fig. 4.16.

The resulting input power compression (IP_{1dB}) and third-order intercept (IIP3) points measured from 4GHz to 24GHz are plotted in Fig. 4.17a. The measured frequency range is limited by the external amplifier's bandwidth. It is expected that large-signal compression and intermodulation characteristics below 4 GHz and above 24 GHz (i.e., from 25 to 43 GHz) do not vary significantly from the measured trends. Measurements predict an average IP_{1dB} of 15.8 dBm and average IIP3 of 25.2 dBm across frequency where the difference is 9.4 dB. Detailed IP_{1dB} (+16 dBm) and IIP3 (+22.5 dBm) behaviors measured at 10 GHz are plotted in Fig. 4.17b. The differential input powers required to reach compression

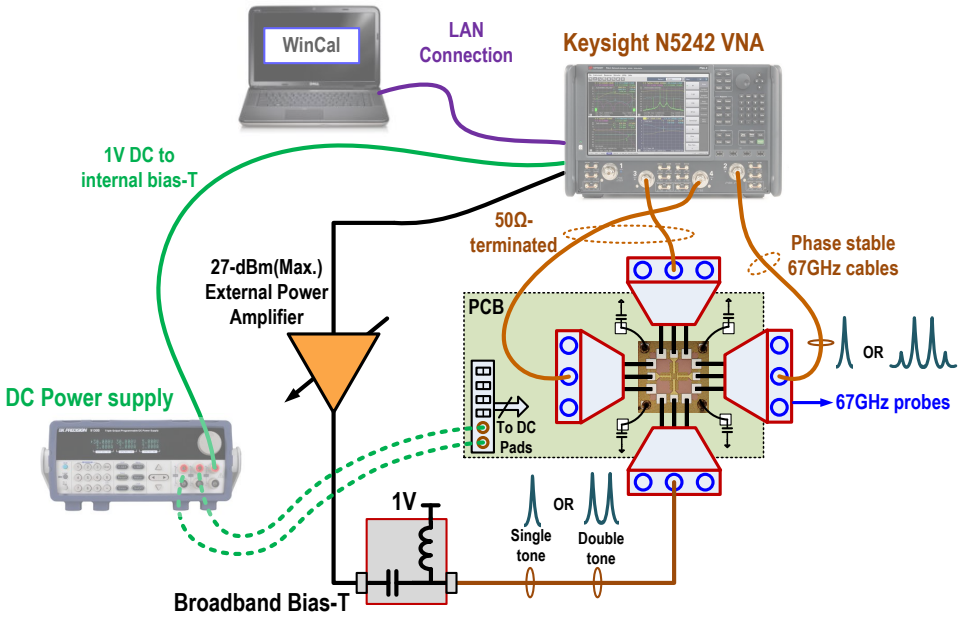


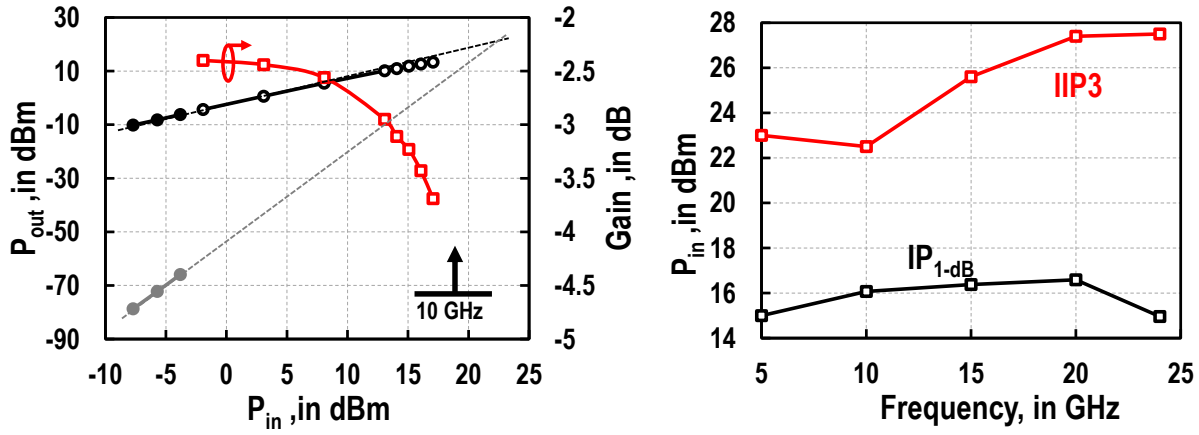
Figure 4.16: Experimental set-up for large-signal measurements

(DIP_{1dB}) and the intermodulation intercept (DIIP3) are 3-dB higher than the single-ended measurements, at +19 dBm and +25.5 dBm, respectively. The simulated IP_{1dB} is +19 dBm at 10 GHz, which is 3-dB higher than the measured IP_{1dB} data.

4.4 High-Isolation 60-GHz SPDT Switch Design

The proposed SPST switch is a circuit building block that is used to develop a tuned, 60-GHz SPDT switch. To characterize the SPDT switch, the number of test ports is constrained to a maximum of 4 (50-Ω) ports. Since the SPDT switch has three differential or 6 single-ended 50-Ω ports, a balun is used at the common port (i.e., antenna port) to transform the differential output to a single-ended port. Moreover, the balun turns ratio can be used to facilitate impedance matching of the switch output to 50 Ω.

Fig. 4.18 shows the proposed SPDT switch circuit schematic diagram. The design adopts 2 fully-differential SPST switches using the proposed SPST switch described in Section 4.1 to 4.3 . Since, the impedance seen by each switch port is capacitive, ports P_1 and P_2 are matched to 100 Ω differentially using series inductors L_{M1} and shunt capacitor C_M, and port P_3 is matched to 50 Ω via a balun (i.e., L_{B1} and L_{B2}) and shunt tuning capacitor



(a) (b)

Figure 4.17: Measured large-signal performance (a) Insertion loss compression at 10 GHz and third-order intercept for 10-GHz and 10.02-GHz input tones (b) Input 1-dB compression of the insertion loss and input third-order intercept point across frequency

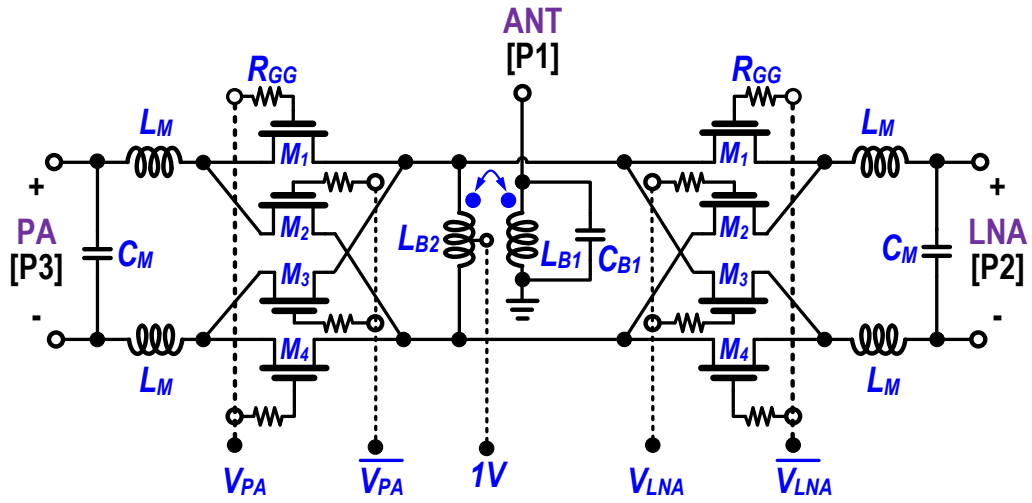


Figure 4.18: Proposed high-isolation SPDT switch schematic diagram

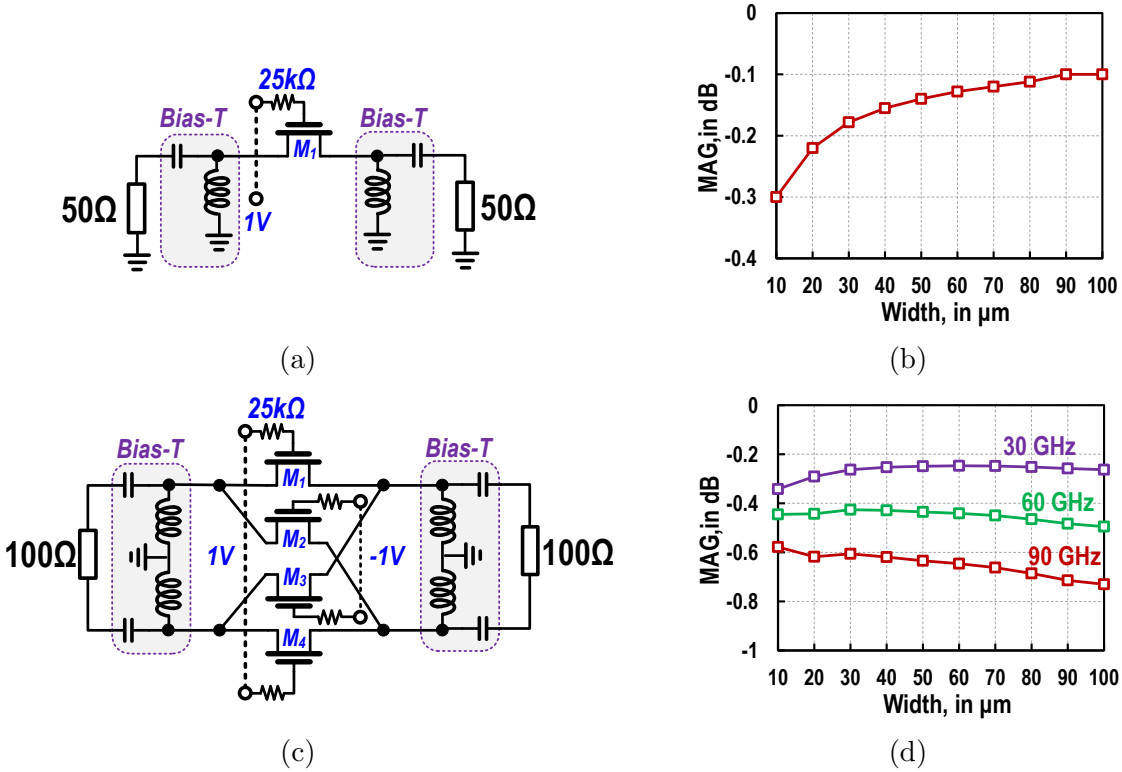


Figure 4.19: Small-signal characterization for floating-body transistors with aspect ratio $W/40$ nm: (a) single series switch schematic, (b) maximum available gain (MAG) simulations for the series switch of part(a), (c) differential SPST switch schematic, and (d) MAG simulations for the differential switch of part(c)

C_{B1}. Transistors M_1 and M_4 have the same transistor aspect ratio, which maximizes isolation in the OFF state. It should be noted that increasing the switch size rises the input capacitance, therefore a smaller inductor value is required when tuning it to the 60-GHz operating frequency.

4.4.1 Transistor Sizing

The SPST switch achieves isolation that is insensitive to transistor sizing by equalizing the substrate coupling across in-phase and anti-phase ports. However, little attention is given to the insertion-loss variation as the transistor width is changed.

Fig 4.19 shows the maximum available gain (MAG) of a conventional series switch and

the proposed SPST switch in a stand-alone 2-port small-signal simulation test-bench across different total device widths, W. The transistors used in the simulation are floating-body devices with an aspect ratio of 1 μm/40 nm. All transistors are RC parasitic-extracted to the highest aluminum metal layer of BEOL stack 18. As expected for the conventional series switch (see Fig. 4.19a, b), the insertion loss decreases with increasing the device width. On the other hand for the differential SPST switch (see Fig. 4.19c, d), the insertion loss is almost constant across width, and increases with increasing frequency. The trend for the SPDT switch follows the analysis shown in Section 4.2.2, where the time constant $R_{on}C_{off}$ is insensitive to the device width, as given by:

$$R_{on}C_{off} = \frac{(C'_{db} \parallel C'_{sb}) + (C'_{gs} \parallel C'_{gd})}{\mu C_{ox}(V_{GS} - V_{TH})}.L, \tag{4.6}$$

where $(C'_{db} \parallel C'_{sb}) + (C'_{gs} \parallel C'_{gd})$ is the equivalent capacitance of a unit transistor. Its minimum value is determined by setting the device length L at its minimum. The insertion loss increases with frequency as expected from Eqn. 4.3. Moreover, the variation of insertion loss across the width is mainly due to the extrinsic RC parasitics of the interconnect metals.

4.4.2 Passive Component Design

The design of passive components for impedance matching at the SPDT switch ports is highly dependent on the device input impedance, which depends on switching device dimensions. As stated in the previous subsection, the MAG of the IL is almost independent of the transistor width, as a result, the selection of width should facilitate matching to single-ended 50-Ω or differential 100-Ω ports. Fig. 4.20 shows the proposed impedance matching plan for the SPDT switch designed in this work. Firstly, the transistor input impedance, with extracted BEOL parasitics, is swept across different width settings. Since R_{on} decreases and C_{off} increases with increasing transistor width, the impedance Z_{SW} moves towards the short circuit point as shown in Fig. 4.20. Matching to 100 Ω is easily achieved by setting the real part of impedance Z_X ($Re\{Z_X\}$) close to 50 Ω (i.e., using a device width of 30 μm (see Fig. 4.20)) and $Re\{Z_Y\}$ close to 100 Ω. As a result, Z_Y can be rotated to the origin of the Smith chart using a series inductor. It should be noted that the best performance is realized when the minimum number of high-Q (i.e., Q exceeds 15 at 60 GHz) passive inductors are used.

The inductance of the balun primary winding L_{B1} at the antenna port is used to transform a 50-Ω port to a differential $Re\{Z_{SW}\}$ load via the secondary winding L_{B2}.

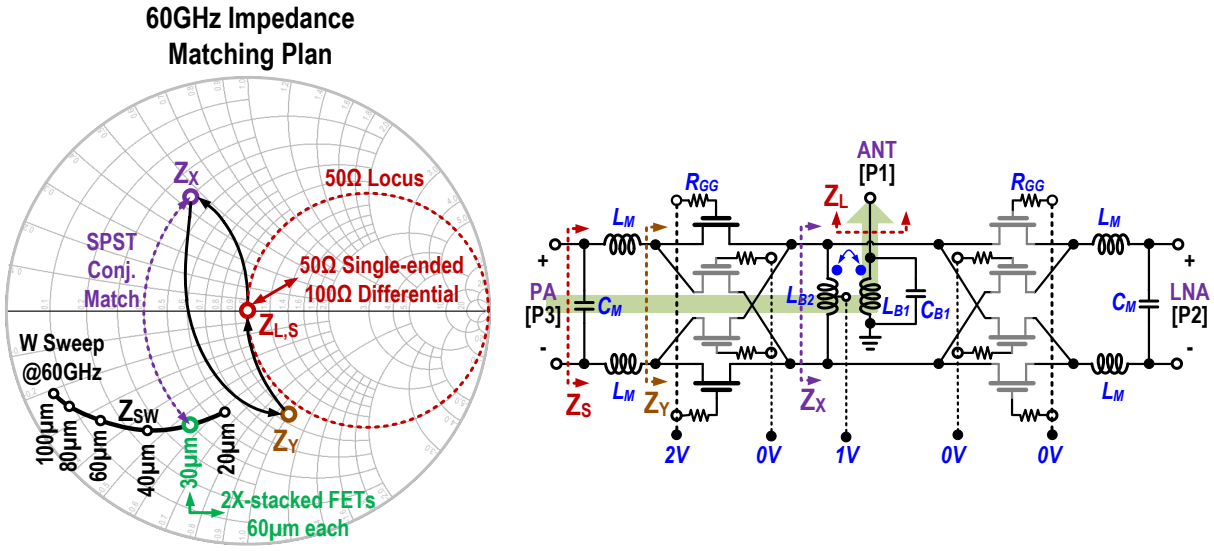
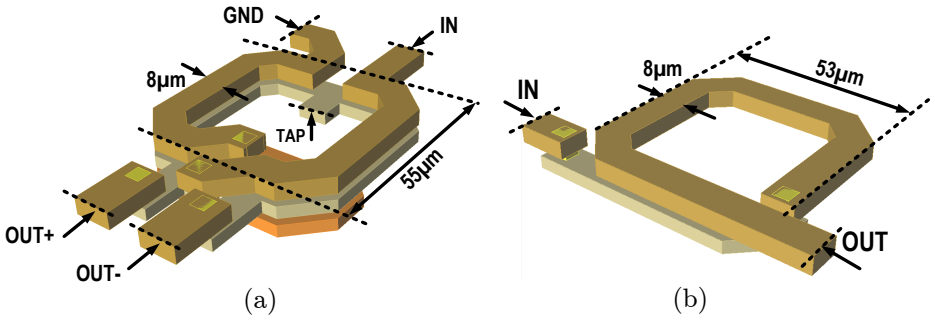


Figure 4.20: 60-GHz impedance matching plan showing impedance rotation across different schematic nodes

The secondary, L_{B2} is shared between two SPST switches. Impedance Z_X is designed to conjugate match to Z_{SW} for maximum power transfer. It is translated to Z_Y by raising the switch input resistance close to 100 Ω. A series inductor L_M is required to tune out the input capacitance of the switch. MIM capacitors C_{B1} and C_M are used to adjust the impedance matching at the three ports, taking into account the parasitic substrate capacitance of the inductors.

Fig. 4.21a, b shows the physical dimensions of the passive inductors designed using the 3 top metal layers (i.e., OA, OB, and LD) of the BEOL stack. Magnetic coupling is realized by stacking inductors to minimize the parasitic capacitance to the substrate. Two stacked floating-body NFET switches with aspect ratios of 60 $\mu m/40$ μm are adopted to improve signal compression characteristics, where the BEOL structure for the terminals is shown in Fig. 4.22.

Fig. 4.23 shows the physical layout for EM simulation of the SPDT active area. The interconnects between switch components increase the overall insertion-loss and perform impedance shifts across circuit nodes, and therefore several EM iterations are required for frequency tuning. Table 4.1 lists a summary of the passive element parameters used in the SPDT switch design.



(a) (b)

Figure 4.21: 3D isometric views (a) antenna port balun (b) single-ended inductor of the PA/LNA ports

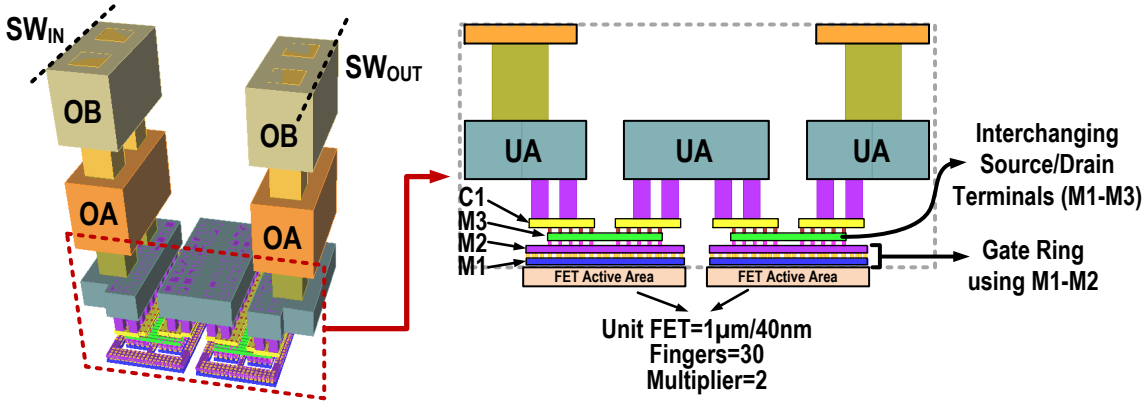


Figure 4.22: 3D isometric view of BEOL stack of a single switch element

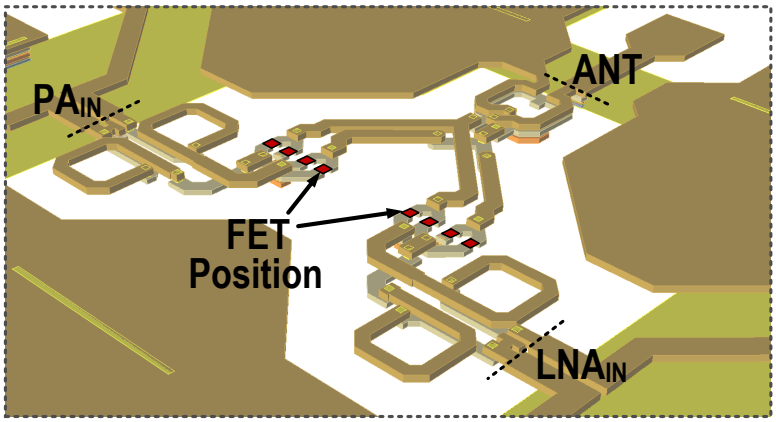


Figure 4.23: Physical layout of the SPDT switch active area for EM simulation

Table 4.1: Passive Component Parameters for the SPDT Switch

Element	Width	Outer dimensions	Inductance[1]	Capacitance	Coupling[1] factor (k)	Q @60G
L_{B1}/L_{B2}	8μm	55μm×55μm	134/87pH	—	0.514	14/22
L_M	8μm	53μm×53μm	152pH	—	—	42.6
C_{B1}	—	10μm×14.5μm	—	38fF	—	540
C_M	—	7μm×9μm	—	15fF	—	550

[1] Simulated at 1 MHz frequency, where parasitic capacitances are negligible

4.4.3 Fabricated Prototype Layout

A die photo of the fabricated prototype is shown in Fig. 4.24. The DC bias at the RF ports is set at 1 V, which is the maximum V_{GS} allowed in the 45-nm technology. The gate control voltage ranges from 2 V in the ON state to 0 V for the OFF state. Large-signal compression is determined by the magnitudes of these voltages, and maximizing the values improves the power compression and intermodulation distortion limits of the SPDT switch. The RF probe pad and feeding lines, with ≈ 0.1 dB loss, are designed to match each port to a 50-Ω termination (or 100-Ω differentially) using the top 4.125-μm thick aluminum layer. The 8-metal BEOL stack (Option 18) in the 45-nm RF-SOI CMOS technology is used. The total active area for the switch is 0.117 mm^2.

4.5 Simulation Results

This section presents the small-signal and large-signal simulation results of the 60 GHz SPDT switch. Furthermore, process, voltage, and temperature variations are simulated at 60 GHz.

Small-signal simulations in the ON state for the SPDT switch are shown in Fig. 4.25. The return loss (RL) at both input and output ports exceeds 10 dB across 55 to 65 GHz. Insertion loss is less than 3.5 dB across the same band in both phase-shift states (i.e., 0° and 180°) with a relatively flat response having just ±0.125 dB variation. Isolation (ISO) simulated in the OFF state is plotted in Fig. 4.26. ISO exceeds 40 dB from 55 to 65 GHz when the switch is driven differentially. Simulated ISO is finite due to a mismatch of transistor parasitics and routing the differential signals of the physical implementation.

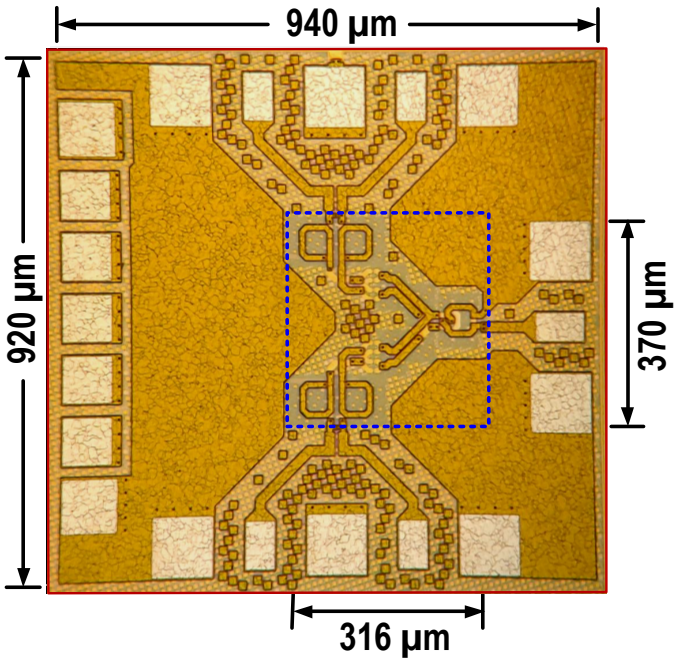


Figure 4.24: Die photo of the fabricated SPDT switch prototype

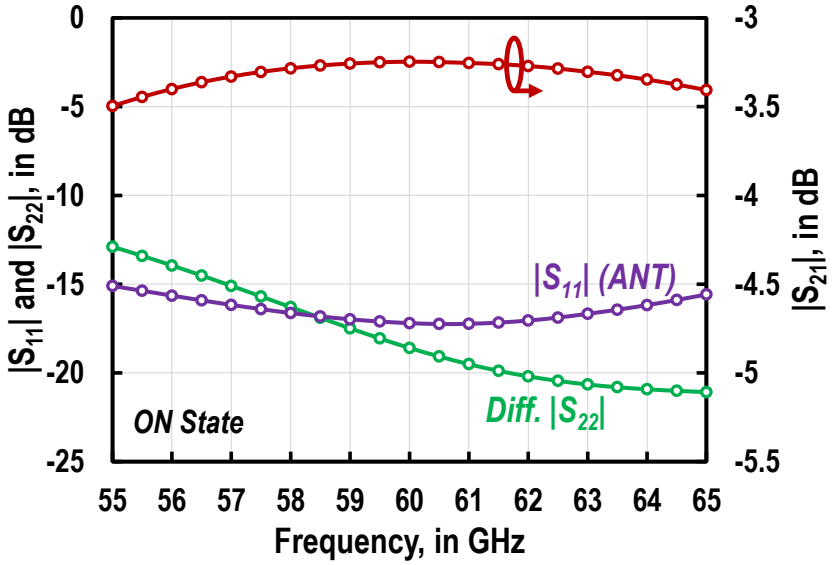


Figure 4.25: Small-signal ON-state simulation results

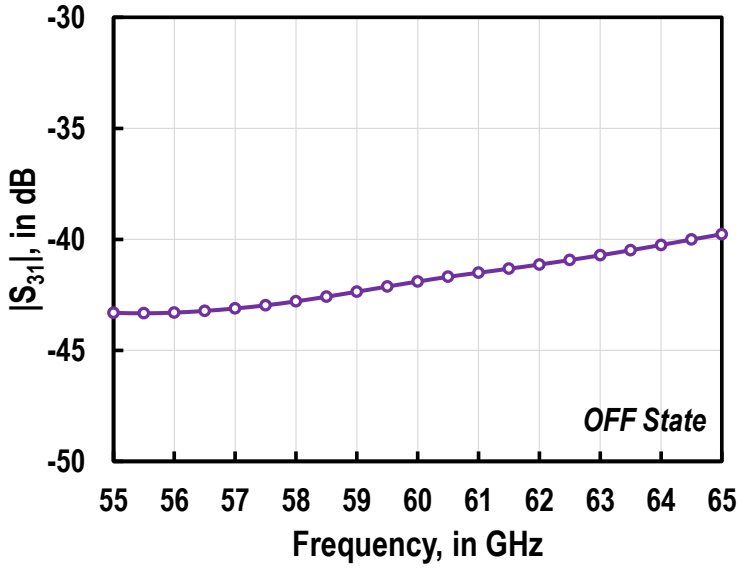


Figure 4.26: Small-signal OFF-state simulation results

Large-signal simulations for the SPDT switch is shown in Fig. 4.27. The input 1-dB compression (IP_{1dB}) and intermodulation intercept point (IIP3) are simulated at 60 GHz using differential excitation at ports 2 while monitoring the insertion loss compression and third-order powers at port 1 (see Fig. 4.20). Simulations predict an IP_{1dB} and IIP3 of +21.5 dBm and +36 dBm, respectively.

Process variations are simulated using Monte Carlo simulations. The results for 500 samples at 60 GHz are shown in Fig. 4.28. The average insertion loss is -3.49 dB with a variation of ±0.15 dB and a standard deviation of 0.045 dB, as shown in Fig. 4.28a, b. The average isolation is -43.8 dB with a variation of ±1 dB and a standard deviation of 0.272 dB, as shown in Fig. 4.28c, d.

Supply variations are carried by simulating the design by varying the supply voltage with ±5%(i.e., 1.9 V to 2.1 V supply). The variation in insertion loss at 60 GHz in response to supply variation is ±0.1 dB. However, isolation is insensitive to supply variations. Changing the simulation temperature from 0°C to 85°C predicts insertion loss and isolation variations that follow the same pattern as the supply variations.

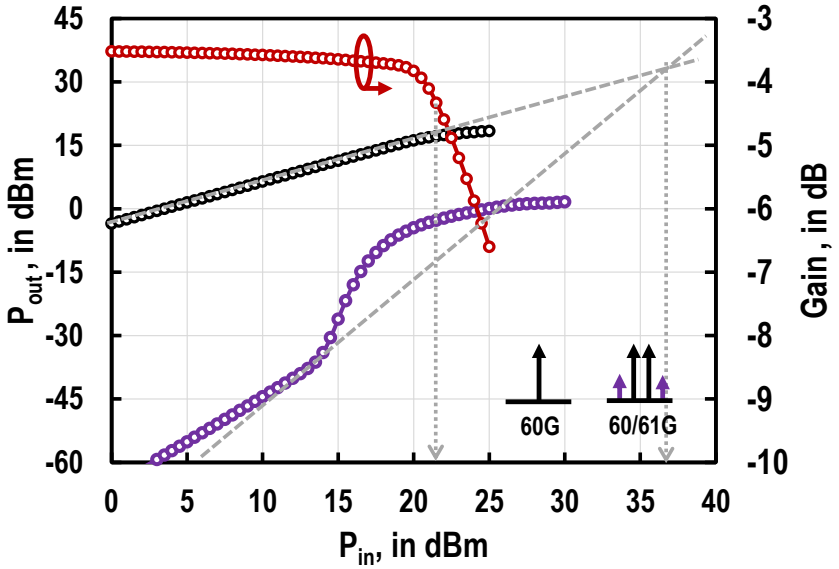


Figure 4.27: Simulated large-signal performance with 60-GHz input tone for gain compression and 60/61-GHz input tones for third-order intercept point

4.6 Literature Comparison

The performance of the SPST prototype is compared to representative examples from the recent literature in Table 4.2. In [71], a shunt inductor is connected to D, S terminals of a floating-body device to synthesize an open circuit at resonance. While simple to implement, the inductor occupies a large area compared to the switch size, isolation performance is inherently narrowband (i.e., 5 GHz), and tuning is susceptible to processing variations. The design proposed in this work realizes at least 20-dB greater isolation than [71] across 43-GHz bandwidth. It also realizes at least 25-dB greater isolation than [72], which is a conventional series-shunt switch topology implemented using the same 45-nm SOI node.

Maximum measured values of the proposed SPST switch for input compression of the IL and the input third-order intercept points are +16.6 dBm (DIP_{1dB}=+19.6 dBm) at 20 GHz and +27.4 dBm (DIIP3=+30.4 dBm) at 20 GHz, respectively, which is comparable to the best results realized for CMOS switches biased from low-voltage (i.e., less than 3 V) supplies. Furthermore, it realizes 12.5 dB larger compression than [72], which is implemented using the same technology node. The capability for 180° phase shifting for the new SPST circuit is also advantageous for phased-array antenna applications, as it relaxes the range required from a dedicated phase shifter.

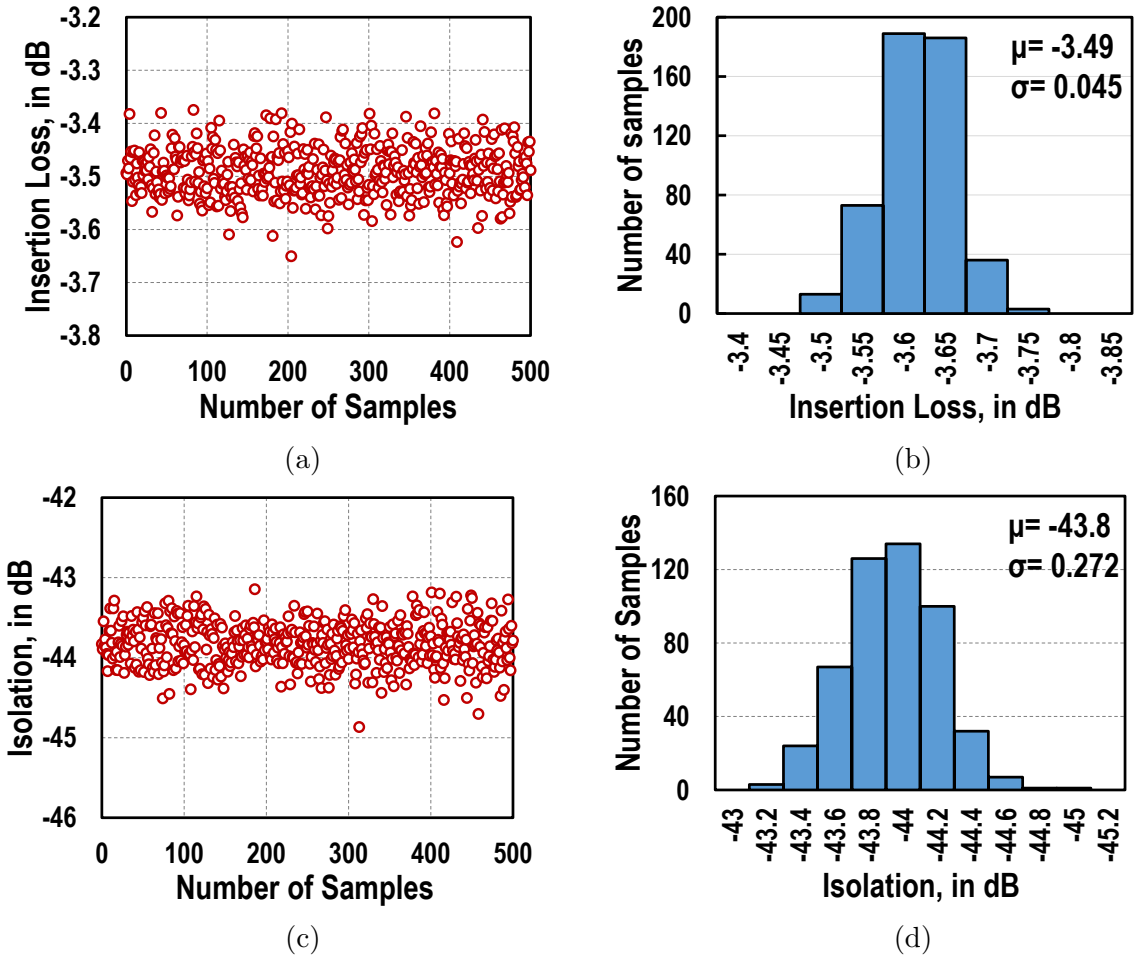


Figure 4.28: Monte Carlo Simulation Results: (a) Insertion-loss random distribution, (b) Insertion-loss mean and standard deviation, (c) Isolation random distribution, and (d) Isolation mean and standard deviation

Simulation results for the proposed SPDT switch are listed in Table 4.2. Small-signal simulations predict an IL of less than 3 dB from 55 to 65 GHz, which is larger than the IL reported in [72] by 0.5 dB at 60 GHz, and equivalent to the reported in [73] at 24 GHz. Isolation remains larger than 40 dB across the 10-GHz bandwidth, which greater than the reported in [72] and [74] by 15 dB and 10 dB, respectively, at the 60-GHz band. Isolation is maintained larger than the reported at different frequency bands from all designs listed in Table 4.2. The SPDT switch predicts an IP_{1dB} of 21.5 dBm, which is larger than the reported at the 60-GHz band in [74] and [72] by at least 11.5 dB. Furthermore, the proposed

SPDT provides a phase shift of 180°, which is not offered by other examples listed in Table 4.2.

4.7 Conclusion

A new, wideband SPST RF switch uses anti-phase RF signal coupling to realize greater than 50-dB ISO in the OFF state across DC to 43 GHz, IL less than 3 dB, and differential IP_{1dB} of +19.6 dBm. Wideband, 60-GHz SPDT switch predicts larger than 40-dB ISO in the OFF state and less than 3.5-dB IL in the ON state from 55 to 65 GHz. Large-signal IP_{1dB} is 21.5 dBm. In addition, Both SPST and SPDT switches facilitate 180° phase-shifting across each switch, which is useful in phased-array transceiver applications.

Table 4.2: Performance Comparison with mm-Wave Switch Designs from Recent Literature

Ref.	Technology	Topology	Freq. (GHz)	I.L. (dB)	R.L. (dB)	ISO (dB)	IP_{1dB} (dBm)	Phase shift (°)	Supply (V)	Area (mm^2)
This Work	45 nm SOI CMOS	Sub. Coupling Compensation SPST	DC-43.5	<3	>10	>50	19.6@20G	180	0/2	0.0058
This Work (Sim.)	45 nm SOI CMOS	Sub. Coupling Compensation SPDT	55-65	<3.5	>10	>40	21.5@60G	180	0/2	0.117
[26] 2019	65 nm (IIIV) CMOS	Asymm. Series Shunt SPDT	25-30	1.16	>15.9	25-30	>5.2@28G	—	0/1	0.01
[75] 2018	65 nm CMOS	Switched Inductor SPDT	25-39.5	1.9	>20	39@28G	7.25	—	0/1.2	0.018
[74] 2017	65 nm CMOS	Transformer based SPDT	65-77	>1.8	>10	22-30	10@66G	—	—	0.015
[72] 2013	45 nm SOI CMOS	Series-Shunt SPDT	DC-60	<3	>15	>25	>7.1	—	0/1	0.04
[73] 2008	90 nm CMOS	Floating Well SPDT	24	3.5	>10	>22	28.7	—	0/1.2	0.018
[71] 2007	130 nm CMOS	Parallel Resonance SPST	25-45	1.8	>20	>30	22	—	—	0.0276

Chapter 5

CMOS Passive Phase Shifter Design

5.1 Introduction

Passive phase shifters are reciprocal networks that can be shared between an LNA and PA in a reconfigurable transceiver. Moreover, they consume no DC power, which is an advantage for low-power applications. However, they usually occupy a larger physical area when compared to active phase shifters, and introduce high insertion loss, especially with increasing phase resolution (as outlined previously in Chapter 2).

The design proposed in this work, shown in Fig. 5.1, targets an insertion loss (IL) of less than 7 dB with less than 2 dB IL variation and smaller than 10 ps group delay deviation across phase shift states with a phase resolution of 11.25° per step. Moreover, during design iterations, the chip area of the phase shifter is kept as small as possible. Figure 5.1 shows a block diagram of the cascaded phase shift blocks realized in this work. The phase shifter consists of 3 blocks, a single-step 90° phase shifter, a distributed 90° phase shifter, and a 180° phase inverter. The phase shifter realizes a uniform response by employing cascaded true-time delay cells of identical phase shifts using binary control. The design is calibration-free, however, it is required to calibrate phase against the process, voltage, and temperature (PVT) corners.

Fig. 5.2 shows the insertion phase states distribution across 360° range. The single-step phase shifter blocks of 90° and 180° target symmetric insertion loss across their by-pass (i.e., 0° phase shift) and phase-shift states of 2 dB each. The distributed 90° phase shifter incorporates an artificial slow-wave transmission line with switched-capacitor network control. The distributed approach is realized using a cascaded true-time delay unit of a π-LC

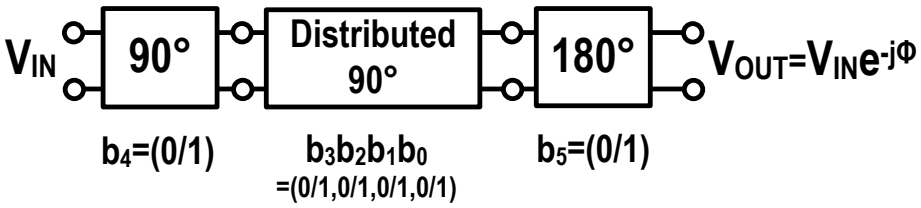


Figure 5.1: Block diagram of the proposed phase shifter

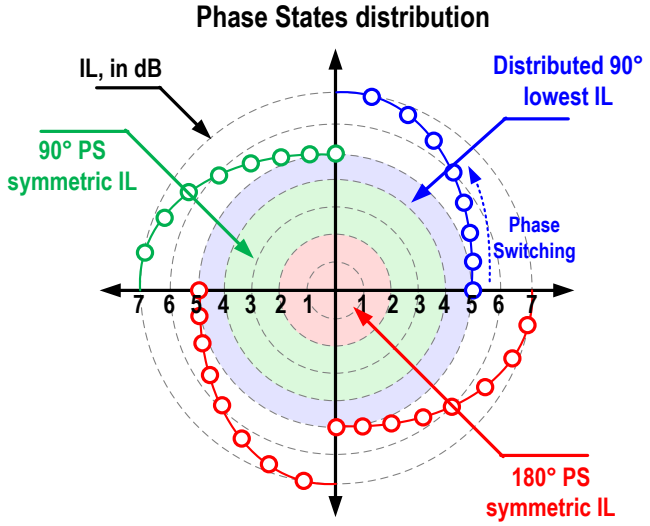


Figure 5.2: Polar diagram showing insertion phase states distribution with insertion loss break down

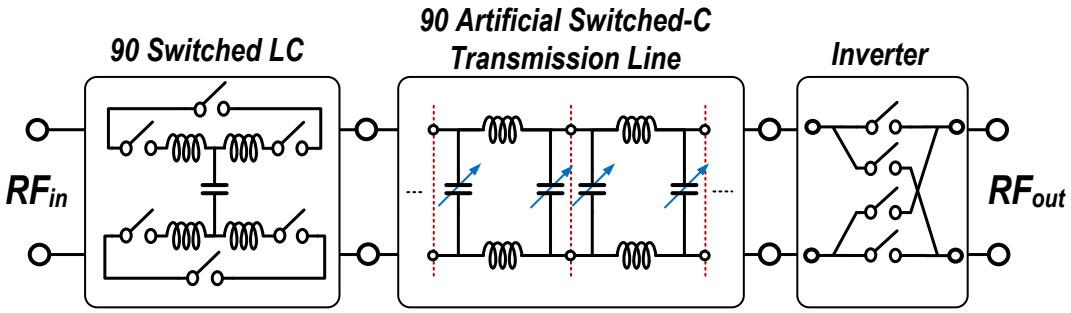


Figure 5.3: Detailed block diagram of the proposed reciprocal passive phase shifter

passive network. The insertion loss introduced is limited by the quality factor of the switched capacitor cell. As a result, the insertion loss gradually increases with increasing the insertion phase shift of the cascaded cells. The target insertion loss of the distributed 90° phase shifter is set between 1 dB and 3 dB as shown in Fig. 5.2. Therefore, the total insertion loss of the phase shifter is expected to change between 5 dB and 7 dB.

The detailed behavioral block diagram of the phase shifter is highlighted in Fig. 5.3. Ground parasitic inductance is avoided by adopting a fully-differential signaling scheme, so the ground plane does not affect the RF signal path and may be completely removed. However, the design has to be fully balanced to minimize insertion loss and phase shift errors due to differential signal imbalance.

A single-step 90° phase shifter is designed using a switched by-pass/LC network [48]. The values of the passive components are determined by the amount of relative phase shift ϕ, the operating frequency ω_o, and the matching impedance Z_o. In the by-pass state, the input and output ports are connected via a by-pass switch, and a relative phase shift of 0° is introduced.

The distributed 90° phase shifter shown in Fig. 5.3 is based on the slow-wave transmission line concept [76]. The total phase shift is broken down into smaller steps, where each step is realized by a true-time delay cell that has a constant group delay for a linear broadband phase shift. A true-time delay switched phase cell is realized using an LC network with a characteristic impedance Z_o of 50Ω. The cell phase can be changed using a switched-inductor network or a switched capacitor network or both. A switched capacitor control scheme is adopted as it is more linear than the switched inductor scheme, since the self-resonance frequency (SRF) of fF-range capacitors are larger than pF-range inductors in the 60-GHz band in the 45-nm SOI-CMOS technology.

The 180° phase shifter with symmetric loss is designed using the SPST switch described in Chapter 3. It is simply implemented by inverting the differential ports such that the output RF signal appears with a 180° phase shift. It should be noted that in a fully reconfigurable transceiver, the 180° phase shift is realized using the SPDT switch as discussed in Chapter 3. Therefore, the total insertion loss of the phase shifter can be further reduced to approximately 3-to-5 dB at 60 GHz.

5.2 Analysis of Phase Shifter Blocks

This section deals with the analysis and design of each phase shifter sub-block to determine values for the circuit parameters. This information is useful as a starting point for more

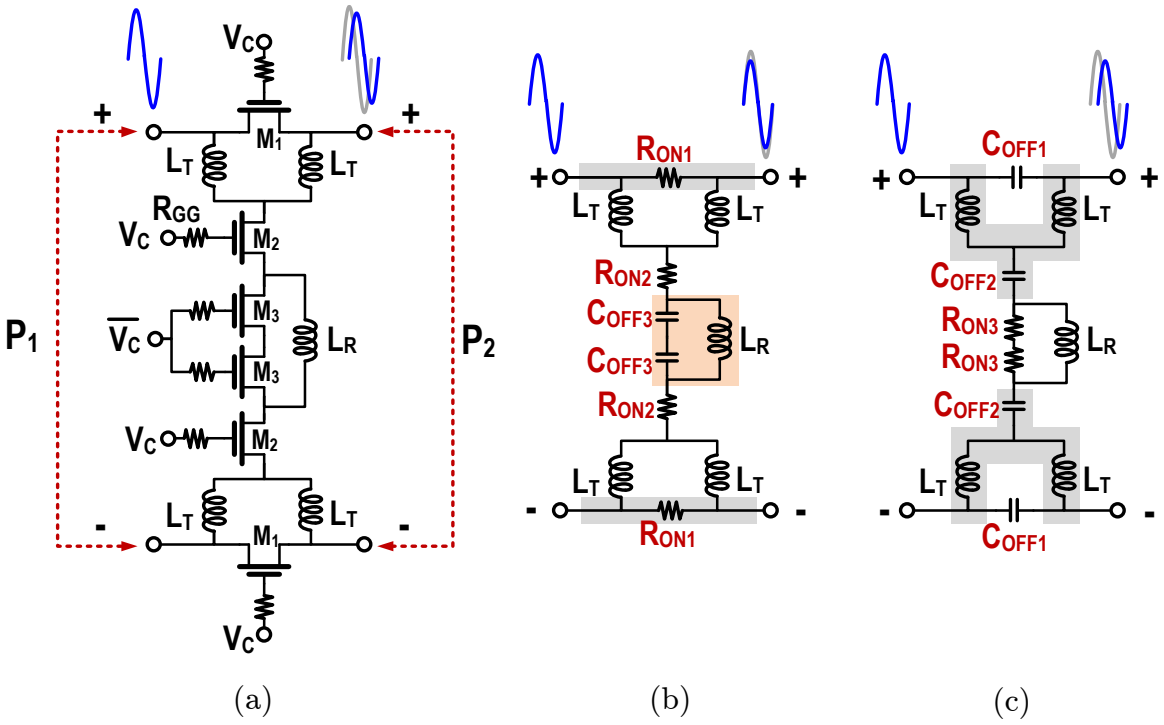


Figure 5.4: Differential switched-LC passive phase shifter (a) circuit schematic (b) by-pass simplified small-signal equivalent circuit (V_c='1') (c) phase shift simplified small-signal equivalent circuit (V_c='0')

detailed simulations and parameter refinement using EM simulation tools.

5.2.1 Single-Step 90° Phase Shifter

Fig. 5.4a shows the circuit design of the 90° phase shifter. The design adopts the single-ended topology described in [48] in a fully differential scheme using lumped inductors. The small-signal equivalent circuit of the by-pass state is shown in Fig. 5.4b. When V_C is ON, the switch by-passes the RF signal to the output port, and the insertion loss is determined by R_{ON1}. The inductor (L_R) resonates with the equivalent OFF capacitance of M_3 ($C_{OFF3}/2$) by creating an open circuit to the virtual ground across f_o, while the input and output ports are shorted together through R_{ON1}. The small-signal equivalent circuit of the phase shift state is shown in Fig. 5.4c, when V_C is OFF. The phase shift is determined by the values of L_T and C_{OFF2} for specific matching impedance Z_o and frequency ω_o .The

parasitic capacitance C_{OFF1} should be small enough to prevent feedthrough to the output port, so any change in phase shift caused by parasitic feedthrough is minimized. The values of L_T, C_{OFF2}, C_{OFF3} and L_R are given by :

$$L_T = \frac{Z_o tan|\phi/2|}{\omega_o}, \tag{5.1a}$$

$$C_{OFF2} = \frac{sin|\phi|}{\omega_o Z_o}, \tag{5.1b}$$

$$C_{OFF3} = \frac{2L_T}{Z_o^2}, \tag{5.1c}$$

$$L_R = \frac{1}{\omega_o^2(C_{OFF3}/2)}. \tag{5.1d}$$

The values of the phase shifter parameters (L_T,C_{OFF2}) are deduced by transforming the ABCD matrix of the corresponding equivalent circuits (neglecting the effect of R_{ON1} and C_{OFF1}) to an S-parameter matrix [77], and then equating $\angle S_{21}$ to the required phase shift. For broadband phase shift (i.e., symmetric group delay), the group delay functions of both states are equalized, leading to the value of C_{OFF3}. For broadband impedance matching, L_R resonates with C_{OFF3} at ω_o.

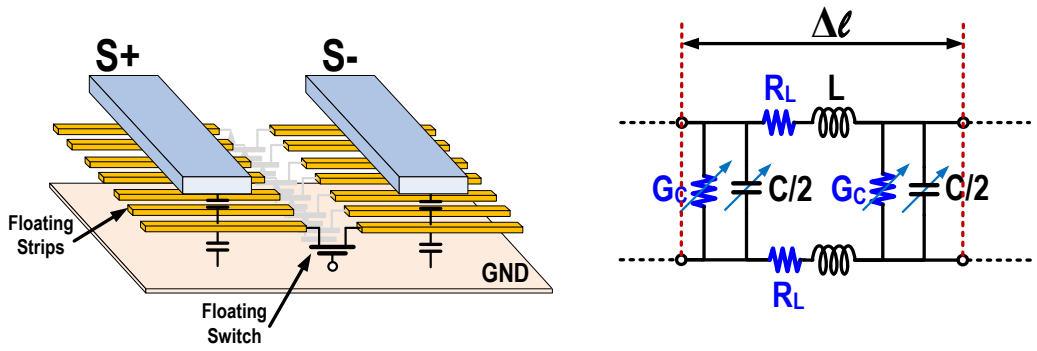
5.2.2 Distributed 90° Phase Shifter

The slow-wave transmission line phase shift approach is shown in Fig. 5.5a [76]. The differential capacitance between S+ and S- (which affects the phase shift) is determined by the state of the floating switches connected to the floating strips, thus changing the electrical length of the transmission line. As a result, a gradual phase shift is achieved while keeping the characteristic impedance Z_c to within ±18% deviation from the port impedance Z_o for a return loss of greater than 10 dB. Using the transmission line theory [54], the propagation coefficient of a repeatable transmission line lumped model (see Fig. 5.5) may be expressed as:

$$\gamma = \sqrt{Z'Y'} = \sqrt{(R' + j\omega L')(G' + j\omega C')} = \alpha + j\beta, \tag{5.2a}$$

$$\alpha = \frac{R'}{2Z_o} + \frac{G'Z_o}{2}, \tag{5.2b}$$

$$\beta \approx \omega\sqrt{L'C'}, \tag{5.2c}$$



(a) (b)

Figure 5.5: Slow-wave transmission line: (a) distributed approach using switched floating strips (b) repeatable-lumped-element equivalent circuit model

where α is the attenuation constant that determines the insertion loss, and β determines the phase shift across the line of length Δl. Assuming that losses are negligible, the characteristic impedance of the transmission line is given by:

$$Z_o = \sqrt{\frac{L'}{C'}}. \tag{5.3}$$

Therefore, for a constant Z_o (of 50 Ω), a ratio of 2500 between L' and C' should be maintained. The phase shift over the line is:

$$\Delta\phi = \beta\Delta l \frac{360^\circ}{2\pi} \approx 360^\circ f_o \Delta l \sqrt{L'C'}. \tag{5.4}$$

By changing the capacitance C' of a nominal 50 Ω line, the maximum allowed step-up/down capacitance values for a broadband return loss of greater than 10 dB is the equivalent to a change in the characteristic impedance to 41 Ω or 59 Ω. Thus, a switched capacitor network that switches the transmission line capacitance per unit length by ΔC/2 can be designed to satisfy the following capacitance range (i.e., C_1 to C_2):

$$C' = \frac{C_1 + C_2}{2}, \tag{5.5a}$$

$$C_1 = C' + \frac{\Delta C}{2}, \tag{5.5b}$$

$$C_2 = C' - \frac{\Delta C}{2}. \tag{5.5c}$$

Fig. 5.5b shows the lumped equivalent small-signal model of a transmission line slice. Parameters R_L and G_C contribute to the slice insertion loss. The phase shift difference over a slice using a switched capacitor network is express as :

$$\phi = \Delta\phi_1 - \Delta\phi_2 \approx 360^\circ f_o \Delta l(\sqrt{LC_2} - \sqrt{LC_1}). \tag{5.6}$$

By designing a single slice that realizes a phase shift of the required resolution, slices can be cascaded to realize a greater phase range without a matching network. It should be noted that as the frequency increases, the inductance and capacitance values required to realize a particular phase shift decrease. As a result, the physical area becomes smaller.

5.3 CMOS Phase Shifter Sub-Block Design

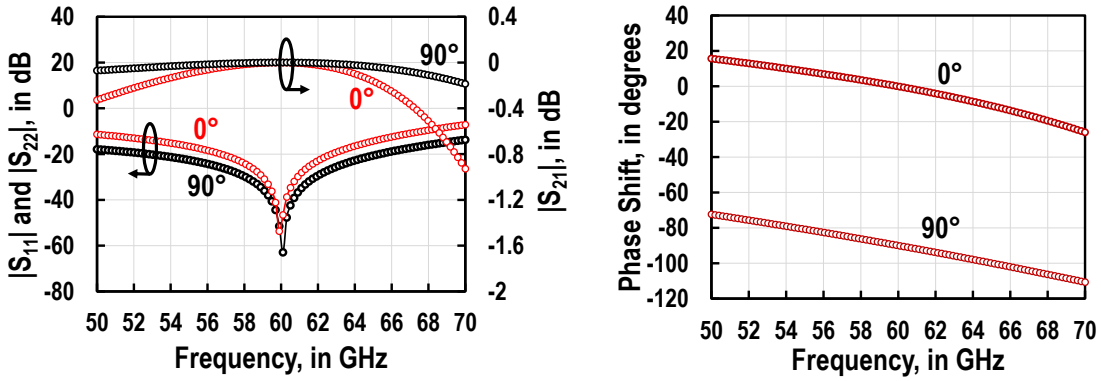
This section discusses the values of the phase shifter parameters at 60 GHz, passive elements design, and layout for the prototype implementation.

5.3.1 Single-Step 90° Phase Shifter

Initial calculations of the phase shifter parameters are shown in Table 5.1. These values are simulated with lossless components, where the results are shown in Fig. 5.6. Both by-pass and phase shift states show wideband matching across 60 GHz with a return loss greater than 10 dB between 50 and 68 GHz. Moreover, the insertion loss shows a wideband response. It should be noted that losses of the inductors, capacitors, and CMOS switches increase the overall insertion loss. Moreover, the parasitic capacitance of the by-pass switch causes the phase to deviate from 90°, so the design values have to account for this variation.

Table 5.1: Passive Component Parameters for Single-Step 90° Phase Shifter

Element	L_T	$C_{off}(M_2)$	$C_{off}(M_3)$	L_R
Value	132.7 pH	53 fF	106.2 fF	66.34 pH



(a) (b)

Figure 5.6: 90° phase shifter small-signal loss-less simulation results: (a) return loss and insertion loss (b) insertion phase

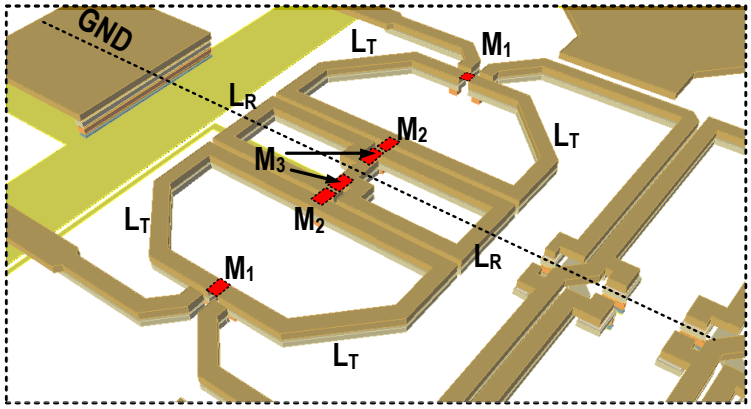


Figure 5.7: EM structure setup showing devices' position and passives used

The design process involves several iterations in the electromagnetic simulation of the phase shifter components. The phase shifter is designed for a 50-Ω impedance seen at input and output ports. However, the RF feeding interconnects cause impedances to shift when connected to other circuit blocks. Therefore, the phase shifter components are designed for smaller than 50 Ω characteristic impedance to absorb the impedance shifts of the feeding lines. As a result, the final values of the phase shift inductance and capacitance are optimized for that purpose.

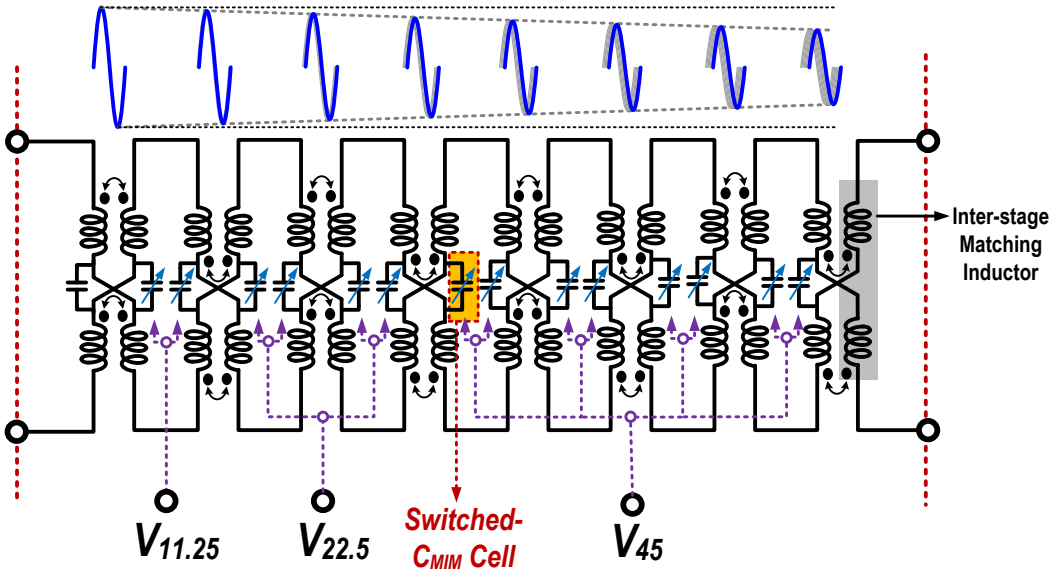


Figure 5.8: Distributed lumped LC 90° phase shifter simplified schematic

Fig. 5.7 shows the EM structure of the single-step 90° phase shifter. The position of the NFET switches is marked in red. The virtual ground centerline of the structure is shown with a dotted line. The inductors are realized by stacking the top metal layers OB and LD to lower the ohmic losses. The widths of transistors M_1, M_2, and M_3 are set to 44 μm, 136 μm, and 160 μm, respectively, while the channel length is set to the minimum of 40 nm for all transistors.

5.3.2 Distributed 90° Phase Shifter

Fig. 5.8 shows the schematic implementation of the lumped slow-wave transmission line. The phase shifter consists of 7 cascaded cells, where each cell represents a π-model equivalent to a 50-Ω transmission line for a reciprocal response. To minimize the physical area of the phase shifter, the in-phase path is interwound with the inverting path so that the magnetic coupling realizes the cell inductance in a smaller area. This implies that the phase shifter can only be excited differentially. Each cell is designed to realize a phase shift of 11.25°. Several EM simulation iterations are required to determine the inductance and capacitance of the π-model that realizes 11.25° phase shift while maintaining the characteristic impedance Z_c at 50 Ω.

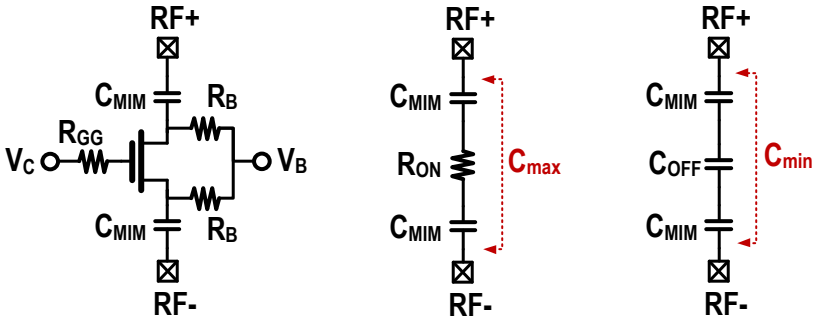


Figure 5.9: Switched capacitor cell design: (a) circuit schematic, (b) high capacitance equivalent circuit, and (c) low capacitance equivalent circuit

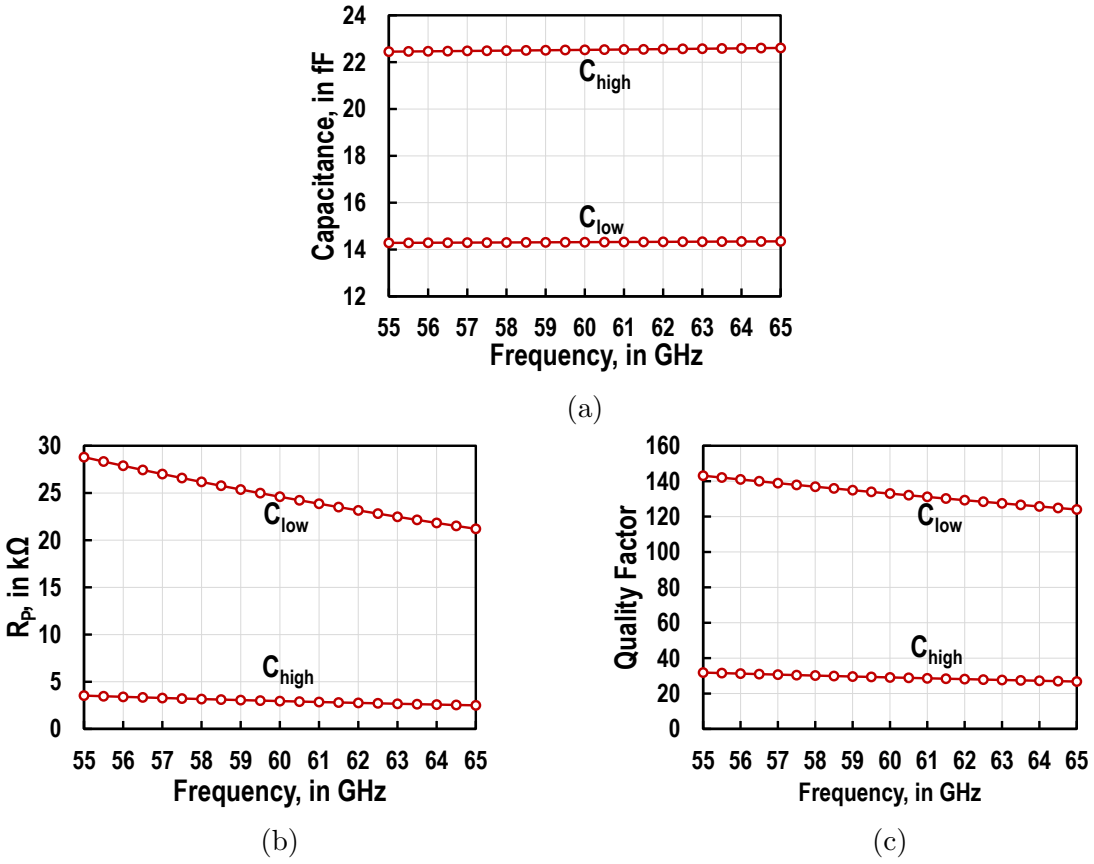


Figure 5.10: Small-signal simulation results of the designed switched capacitor cell: (a) capacitance, (b) parallel resistance, and (c) quality factor

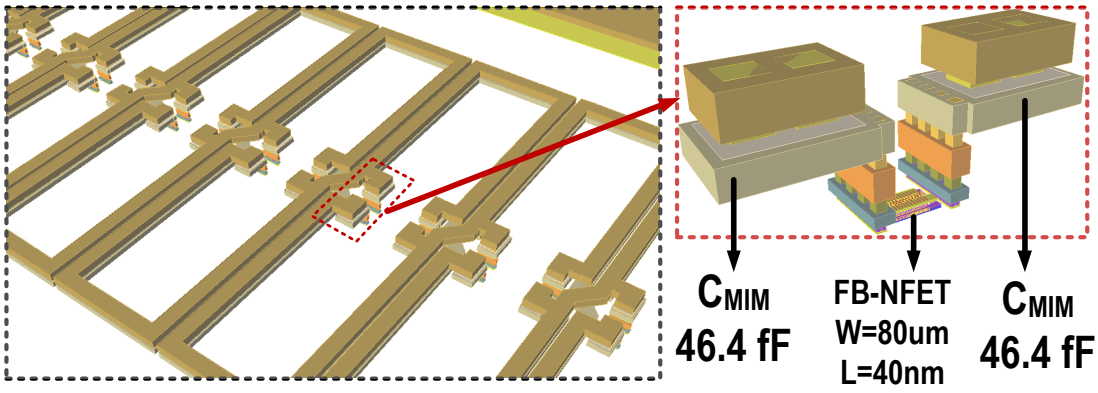


Figure 5.11: EM structure setup of the distributed 90° phase shifter including the switched capacitor cell design

Fig. 5.9a shows the design of the differential switched capacitor cell that is adopted twice in the π-model of the phase shifter cell. The distributed slow-wave approach is avoided, as it occupies a relatively larger area in silicon for a particular phase shift. The design incorporates 2 floating MIM-capacitors with a floating NFET switch. When the switch is ON as shown in Fig. 5.9b, the equivalent capacitance is set to $C_{MIM}/2$. However, the quality factor of the capacitor is reduced by the ON resistance of the switch. When the switch is OFF, as shown in Fig. 5.9c, the equivalent capacitance is set to $(C_{MIM}/2 \parallel C_{off})$. For large-signal (i.e., compression) considerations, the D and S terminals of the NFET switch are biased to 1 V through V_B (see Fig. 5.9a), while the G terminal changes between 0 V and 2 V. Therefore, the switch compression is limited by the ON-state condition, when the RF signal at either D or S terminals exceeds a peak of 1.4 V (assuming V_{th} of the NFET device is 0.3 V).

The small-signal equivalent capacitance, quality factor (Q), and parallel resistance (R_p) of the switched capacitor cell are shown in Fig. 5.10. The differential capacitance changes between 14.3 fF to 22.5 fF, with an average value of 18.4 fF. As a result, for an equivalent 50-Ω transmission line, the inductance required is 184 pH for both in-phase and inverting paths to realize an 11.25° phase shift. This inductance is realized in a smaller physical area by adopting the physical layout shown in Fig. 5.11.

Fig. 5.11 shows the EM structure of the distributed 90° phase shifter with emphasis on the switched capacitor cell. The switched capacitor cell is realized using 2 MIM capacitors of 46.4 fF each and a floating-body NFET of 80-μm width and 40-nm length. Several EM iterations are required to adjust the target inductance for realizing the required phase shift.

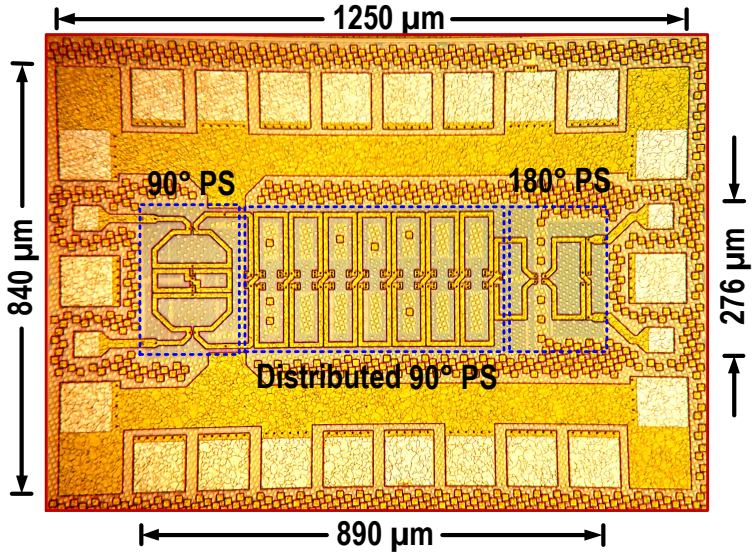


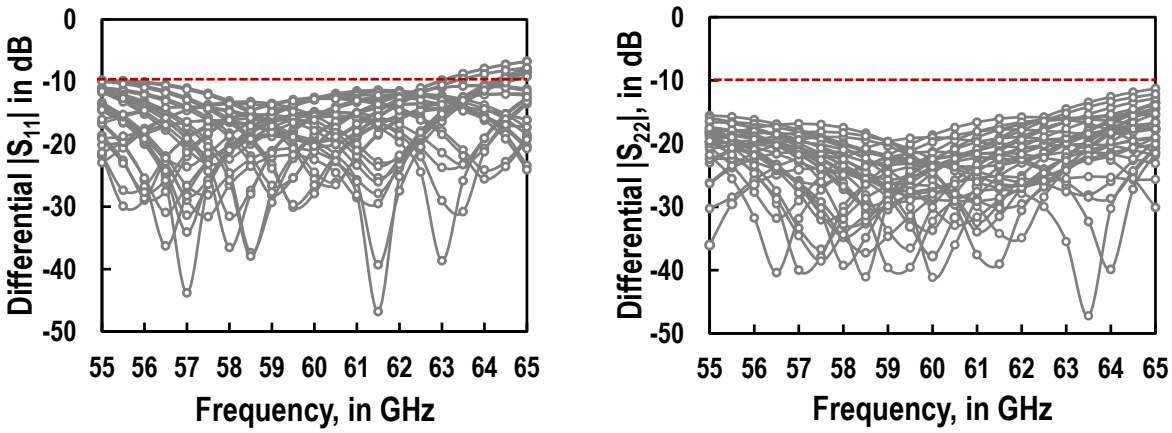
Figure 5.12: Die photo of the fabricated 360° passive phase shifter

5.3.3 Single-step 180° Phase Shifter

The design flow of the 180° phase shifter is the same as that introduced for the SPST switch in Chapter 4. It consists of 4 FB-NFET transistors, each is 24-μm wide. Each single-ended port is matched to 50 Ω using a series 194-pH inductor. It should be noted that in a complete phased-array transceiver system, the 180° phase shifter can be employed using the proposed SPDT switch in Chapter 4. As a result, the total insertion loss of the phase shifter can be reduced by ≈ 2 dB.

5.4 Fabricated Prototype Layout

A die photo of the fabricated prototype is shown in Fig. 5.12. The DC bias at the RF ports is set at 1 V, which is the maximum V_{GS} allowed in the 45-nm technology. The gate control voltage of all switches changes between 2 V in the ON state and 0 V in the OFF state. The large-signal compression is determined by the magnitudes of these voltages, and choosing maximum values improves the power compression and intermodulation distortion limits of the phase shifter. The floating D and S terminals of the switched-capacitor cell are tied to 1 V for the same purpose. The RF probe pad and feeding transmission-lines, with ≈ 0.1 dB loss, are designed to match each port to 100 Ω (differentially) using the top 4.125-μm



(a) (b)

Figure 5.13: Small-signal return loss simulation results of the phase shifter (a) S_{11} (b) S_{22}

thick LD aluminum layer. The 8-metal BEOL stack (Option 18) in GlobalFoundries 45-nm RF-SOI CMOS technology is used for the implementation. The total active area of the phase shifter is 0.245 mm^2.

5.5 Simulation Results

Fig. 5.13 shows the differential return loss simulation results for input (port 1) and output (port 2) ports across all phase shift states. Simulations predict a wideband return loss of greater than 10 dB across the 55-65 GHz band. As a result, the phase shifter can be shared between the transmitter PA and receiver LNA in a mm-wave transceiver.

The differential insertion loss simulated across all phase shift states is plotted in Fig. 5.14. The simulated average insertion loss (IL) is 5.3 dB at 60 GHz. The IL varies between 5 dB at 55 GHz and 6.5 dB at 65 GHz, showing excellent IL flatness across 10-GHz bandwidth. The IL variation across states at 60 GHz ranges between 4.6 dB and 6.1 dB. This small change (i.e., 1.5 dB) facilitates the design of a compensating variable-gain amplifier that can be part of transmitter PA or receiver LNA. The rms error of the IL is less than 1 dB across the entire 55-65 GHz band.

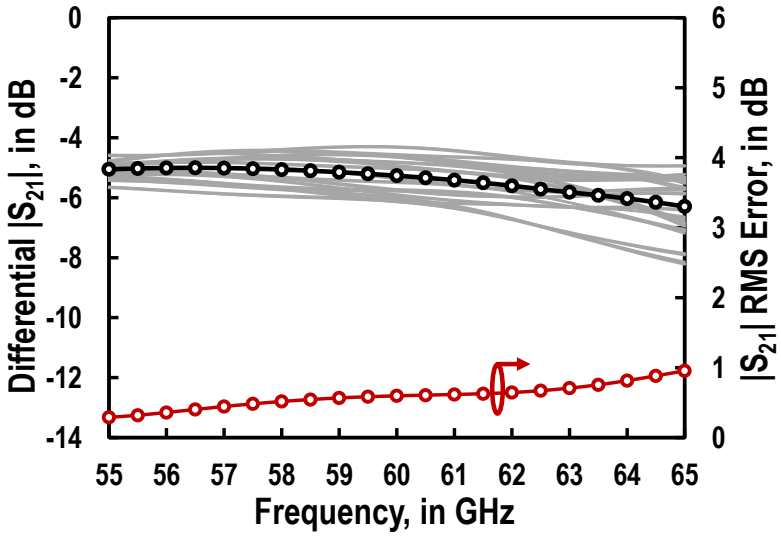
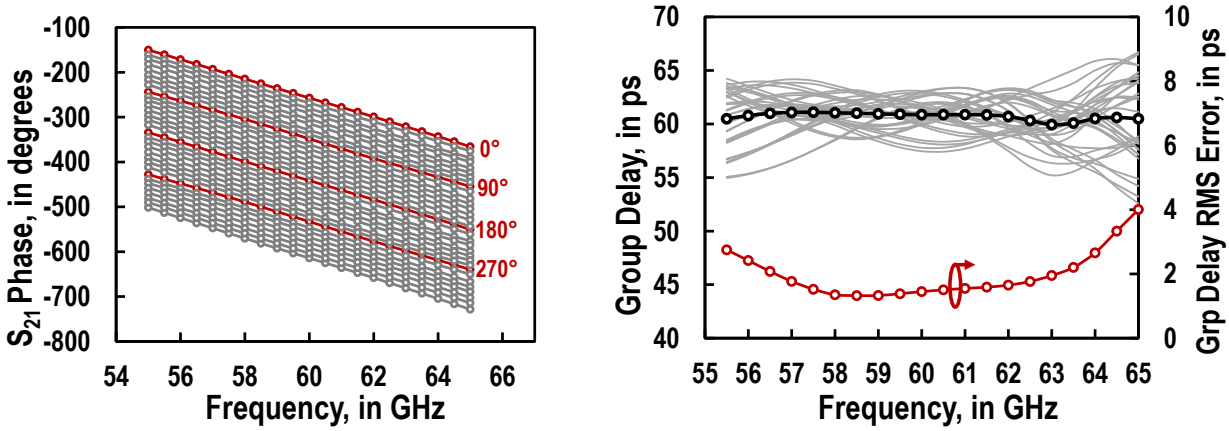


Figure 5.14: Small-signal insertion loss simulation results of the phase shifter across all states with rms IL error



(a) (b)

Figure 5.15: Small-signal insertion phase simulation results of the phase shifter across all states (a) $\angle S_{21}$ (b) group delay

Fig. 5.15a shows the insertion phase across all phase states for the 55-65 GHz band. The phase shifter 5-bit control signals are swept, showing excellent linear phase shift response with 11.25° phase resolution. The red lines highlight the single-step phase shifters of 0°,

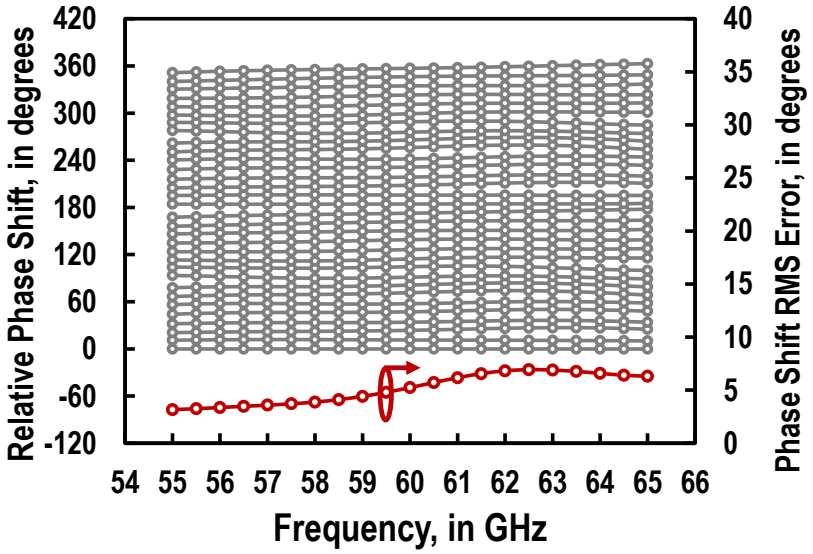
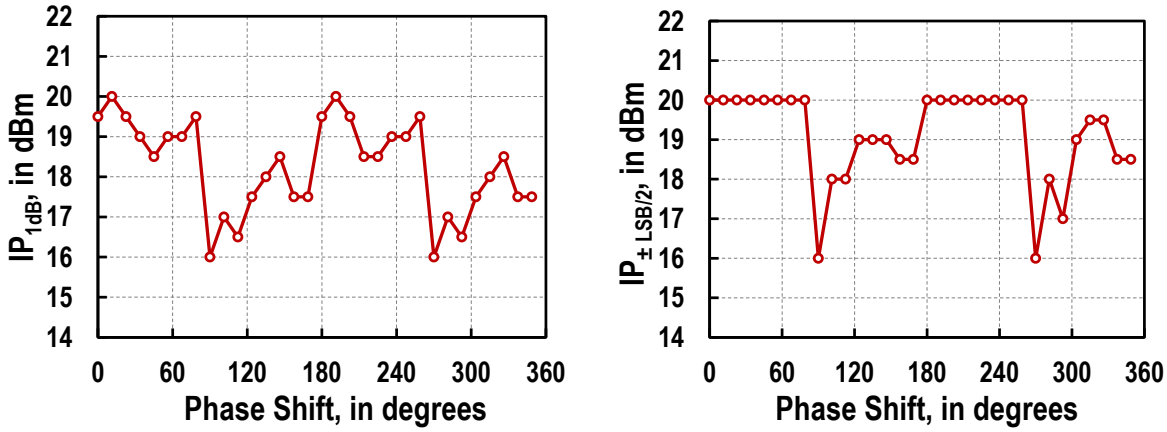


Figure 5.16: Small-signal relative phase shift simulation results of the phase shifter across all states with rms phase error

90°, and 180°. The insertion phase is further assessed by plotting the group delay response across all phase states, as shown in Fig. 5.15b. The simulated average group delay at 60 GHz is 61 ps with smaller than 2 ps group delay deviation across 55-65 GHz band. The group delay variation ranges between 57.5 ps to 63 ps at 60 GHz, and the group delay rms error is smaller than 4 ps across 55-65 GHz.

Fig. 5.16 shows the relative phase shift across all states. The phase shift states cover the 360° range with 11.25° steps. Phase shift rms error is more representative in terms of the phase quality. The rms error is calculated from the deviation of the simulated phase shift from its ideal response across each frequency. Simulations predict smaller than 7° rms error across all states for the entire frequency band. These results predict that the phase shift error is smaller than 1 LSB. As a result, each control word corresponds to one particular phase shift value with no overlap between ± 1 LSB phase shift values.

Fig. 5.17a shows the results for large-signal simulations of the 1-dB gain compression point across all phase states at 60 GHz when driving port 1 (i.e., closer to the single-step 90° phase shifter). The minimum input power compression is predicted at 16 dBm when the phase shift is 90° or 270°, and the maximum input power compression is 20 dBm when the phase shift is 11.25° or 191.25°. The minimum and maximum IP_{1dB} values of the phase shift are limited by the switches M_1, M_2, and M_3 (see Fig. 5.4) of the 90° phase shifter,



(a) (b)

Figure 5.17: large-signal input compression across all states at 60 GHz when driving port 1: (a) 1-dB gain compression (b) ±0.5 LSB phase compression

which experiences early compression compared to the other phase shifter sub-blocks in the chain under large-signal excitation. These results predict excellent linearity performance compared to literature. In this work, a new linearity definition is introduced that is related to phase compression. Fig. 5.17b shows the input power that corresponds to the phase shift compression by ±LSB/2 at 60 GHz. Phase states that reach an input power of 20 dBm are phase compressed at greater than or equal 20 dBm. This means that the phase compression of some states hasn't been noticed for power levels below 20 dBm. The minimum input power for phase compression is 16 dBm when the phase shift is 90° or 270 °. Based on simulations, the 90° phase shifter limits the linearity performance compared to other blocks. If larger power handling is required, device stacking may be adopted to boost the early compression of the 90° phase shifter.

Large-signal compression is simulated at port 2 (i.e., closer to the 180° phase shifter) and predicts an IP_{1dB} of ≈18.5 dBm across all phase states. Phase compression is not noted up to 20 dBm power sweep. Simulations predict that the large-signal performance when driving port 2 is limited by the 180° phase shifter. However, device stacking may be used to increase power handling, if required.

5.6 Literature Comparison

The performance of the proposed phase shifter and other designs from recent literature are listed in Table 5.2 for comparison. The phase shifter is fabricated in 45-nm SOI-CMOS using BEOL option 18. The input and output ports are wideband matched to 100 Ω, with a simulated return loss of greater than 10 dB across 55 to 65 GHz. This bandwidth is larger than that of most other designs operating in the 60-GHz band. The phase shifter is digitally-controlled by a 5-bit word giving 11.25° phase resolution, which is the smallest resolution among other designs with an rms phase error of smaller than 7°. The average insertion loss of the complete network is 5.3 dB with a smaller than 1 dB rms IL error. This insertion loss is the best among the designs listed in Table 5.2, where comparable insertion loss is achieved at larger phase resolution (as in [47, 50]), or larger insertion loss is realized at the same phase resolution, as in [48]. The simulated large-signal P_{1dB} of the phase shifter for a differential input is 16 dBm, and is limited by port 1. Large-signal performance is the best among the passive designs, with smaller than 12 dBm, as in [50]. The active physical area of the prototype is 0.245 mm^2, which is comparable to the other passive designs listed in Table 5.2.

5.7 Conclusion

This chapter discusses the design and implementation of a fully differential wideband 360° passive phase shifter at the 60-GHz band. The proposed design adopts a 90° switched-LC network, a distributed 90° slow-wave switched-C network, and a phase inverter. The simulated average IL is 5.3 dB with a smaller than 1 dB rms IL error. The resolution of the phase shift is 11.25° with smaller than 7° rms phase error. The fabricated prototype consumes an active area of 0.245 mm^2 using BEOL metal stack option 18 of the 45-nm SOI-CMOS technology.

Table 5.2: Performance Comparison with mm-Wave Phase Shifters from Recent Literature

FOM	[47]	[48]	[49]	[50]	[52]	[53]	This Work(Sim.)
Tech.	45nm-SOI CMOS	90nm CMOS	65nm CMOS	40nm CMOS	0.13μm SiGe BiCMOS	90nm CMOS	45nm-SOI CMOS
Topology	Switched HP/LP Network	Switched T-LP Network	Switched HP/LP Network	Switched HP/LP Network	Active Vector Sum +LNA	Active Vector Sum	Switched-LC/ Slow-wave Network
Freq. (GHz) (S_{11}<-10dB)	60-67	57-64	57-66	22-36	60-80	58.8-64.3	55-65
Phase Resolution (°)	45	11.25	22.5	45	22.5	22.5	11.25
RMS Phase Error (°)	<3	<10	<5.5	<12.8	<9.1	<10	<7
Gain (dB)	-6	>-18	-8.7±1.7	-5.6±0.5	<14.7	<1.1	-5.3
RMS Gain Error (dB)	<1.3	<1.8	<1.17	<0.6	1.3	<1.6	<1
Input P_{1dB} (dBm)	6	—	7.4	<12	-27	-9.8±0.8	16
Supply Voltage (V)	0/1	0/1.2	0/1	0/1	3	1.8	0/2
DC Power (mW)	0	0	0	0	108/34.8	19.8	0
Active Area (mm^2)	0.3	0.34	0.092	0.132	1.06	0.61	0.245

Chapter 6

CMOS Low-Noise Amplifier Design

6.1 Introduction

A wideband, low-noise amplifier (LNA) of a CMOS receiver is essential in phased-array beamforming front-end radios. Based on the link-budget analysis of wireless up-link/down-link deployment scenarios, a low-noise operation is essential to minimize contribution to the thermal noise floor. Moreover, enough power gain is required to account for insertion loss (IL) of the single-pole, double-throw (SPDT) switches connected to the amplifier and to achieve the required signal-to-noise (SNR) ratio of the receiver sensitivity. Additionally, the amplifier should consume minimal DC power consumption (i.e., less than 30 mW) required for low-power wireless handset applications. Moreover, LNAs should provide sufficient linearity to prevent RF signal compression and harmonic distortion across later blocks in the receiver chain.

Based on the specifications introduced in Chapter 1, the LNA should provide a forward gain of 20 dB, wideband matching across 57-64 GHz or larger, a noise figure of 3 dB with minimum variation across the same band and at the lowest possible power consumption, and occupying the smallest physical area. The proposed design flow is outlined as follows. Firstly, selected devices from the 45-nm SOI-CMOS technology are characterized for low noise and high gain including layout parasitics. Secondly, a 2-stage amplifier topology is introduced which is designed for simultaneous noise and power matching at the input. A summary of the passive component designs developed for the LNA implementation is then summarized. Top-level simulation results are presented with input and output ports matched to 50-Ω terminations (i.e., 100 Ω differentially). Simulation results are then

presented. Finally, the LNA performance is compared to designs reported in the recent literature.

6.2 A 2-stage, 60 GHz Low-Noise Amplifier Design

This section provides details on the common source NFET transistor characterization, impedance noise and power matching plan, a 2-stage amplifier design including transistor sizing and passive components design, and the layout of the fabricated prototype.

6.2.1 Device Characterization for Noise and Gain Performance

The 45-nm SOI-CMOS technology offers several FET devices optimized for different applications. Among these devices, the floating-body (FB) NFET device has a lower noise figure than the body-contact (BC) transistors. This is primarily attributed to the increased gate-electrode resistance of BC transistors compared to FB transistors [78]. Although FB devices exhibit the kink effect in their DC I-V characteristics [79], this does not affect the linearity of the LNA at lower received power levels (i.e., below -60 dBm). A single transistor aspect ratio of 1 μm/ 40 nm is chosen and a double-contacted gate is used in the transistor layout to minimize the extrinsic gate resistance, which is an unwanted source of thermal noise.

Fig. 6.1 shows simulation results of the minimum noise figure (NF_{min}) at 60 GHz for a common-source FB-NFET with changing V_{GS} and V_{DS}. The device achieves its minimum noise figure of 1.4 dB when $V_{GS} = 0.4 \approx 0.5$ V and $V_{DS} = 1$ V. Moreover, as V_{DS} decreases, the minimum noise figure becomes a stronger function of V_{GS} as the threshold voltage V_{TH} is approached. Also, NF_{min} increases by 0.2 dB as V_{DS} decreases from 1 V to 0.5 V Since a 2-stage amplifier is designed to realize the desired overall gain of 20 dB, low-noise operation in the first stage is required to minimize the input-referred noise figure. Furthermore, minimizing DC power consumption is also important for wireless handset applications consuming less than 30 mW. For this purpose, a V_{GS} of 0.5 V and a V_{DS} of 1 V are selected. This operating point realizes an NF_{min} of 1.4 dB, a DC power density (P_{DC}/W) of 270 μW/μm, and an intrinsic power gain of 10.43 dB at 60 GHz.

Fig. 6.2 shows a DC simulation of the FB-NFET for V_{GS} and V_{DS} swept from 0.3 V to 0.7 V and 0.5 V to 1 V, respectively. This simulation is used to predict the current density required for the minimum noise figure and the expected power consumption of the overall

amplifier. Based on a $V_{GS} = 0.4 \approx 0.55$ V (i.e., for NF_{min} to remain below 1.5 dB), I_{DS} consumed by a 1-μm wide device from a 1-V supply ranges between 150 μA to 350 μA.

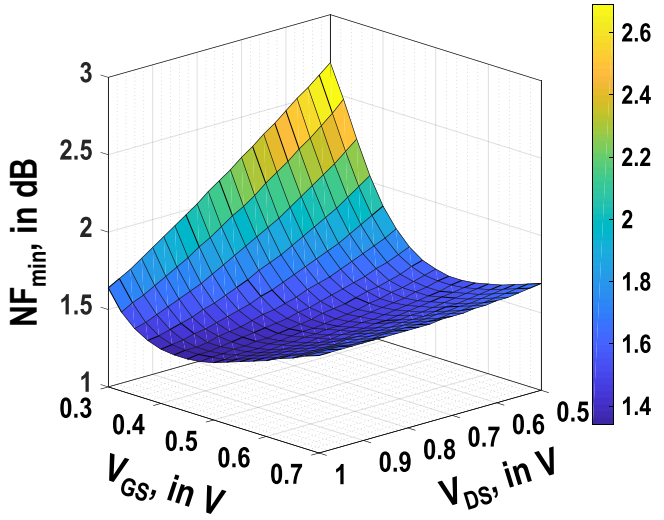


Figure 6.1: Minimum noise figure (NF_{min}) for a floating-body NFET device of aspect ratio 1 μm/40 nm at 60 GHz with V_{GS} and V_{DS} sweep

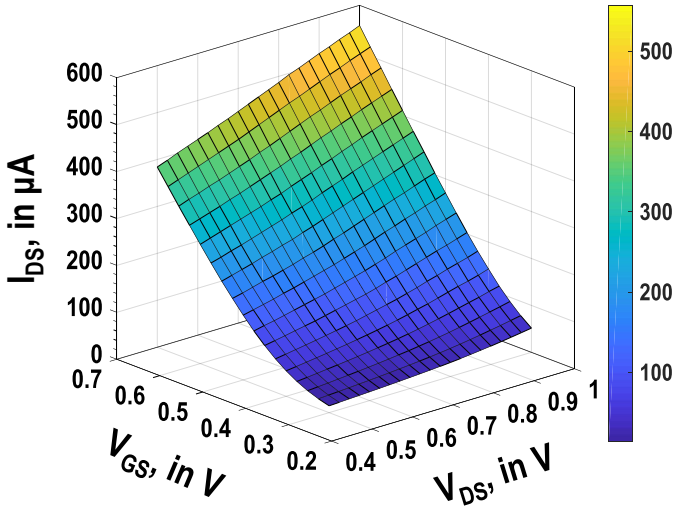


Figure 6.2: D-to-S current (I_{DS}) for a floating-body NFET device of aspect ratio 1 μm/40 nm at 60 GHz with V_{GS} and V_{DS} sweep

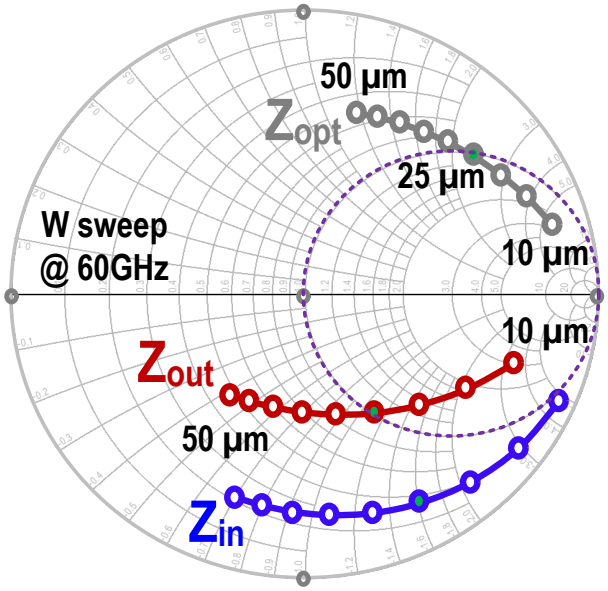


Figure 6.3: FB-NFET device 60-GHz small-signal simulation for Z_{in}, Z_{out}, and Z_{opt}

A small-signal simulation for input, output and optimum noise impedances (Z_{in}, Z_{out} and Z_{opt}) at 60 GHz of a common-source transistor for different transistor width (10 μm to 50 μm) in a 50-Ω system is shown in Fig. 6.3. For stand-alone LNA characterization, $Re\{Z_{opt}\}$ is set close to 50 Ω for noise matching by choosing a device width of 25 μm biased at the optimum current density for the lowest NF_{min}. The real part of the input impedance (i.e., $Re\{Z_{in}\}$) is set to 50 Ω by adding a source degeneration inductor L_s to increase the input resistance by ωL_s. A gate inductor in series with the gate is used to simultaneously match the transistor for maximum power transfer and minimum noise figure to a 50-Ω signal source (i.e., simultaneous noise/power match). The output impedance is matched to 50 Ω by tuning the output impedance Z_{out} at 60 GHz using drain inductor. A floating capacitor may be used for impedance matching and DC power blocking to the output port. This matching methodology is only valid for a single-stage amplifier. A multi-stage amplifier design requires conjugate inter-stage matching, so gain circles (i.e., impedance circles where the gain is constant) vs. noise circles (i.e., impedance circles where noise figure is constant) are a better representation to illustrate the compromise between gain and noise performance when matching is performed across stages.

Fig. 6.4 shows the noise and gain circles of a 20-μm wide FB-NFET transistor in the common-source configuration at 60 GHz biased at 270 μA/μm. Each circle corresponds to a range of impedances where noise figure (NF) and maximum available power gain

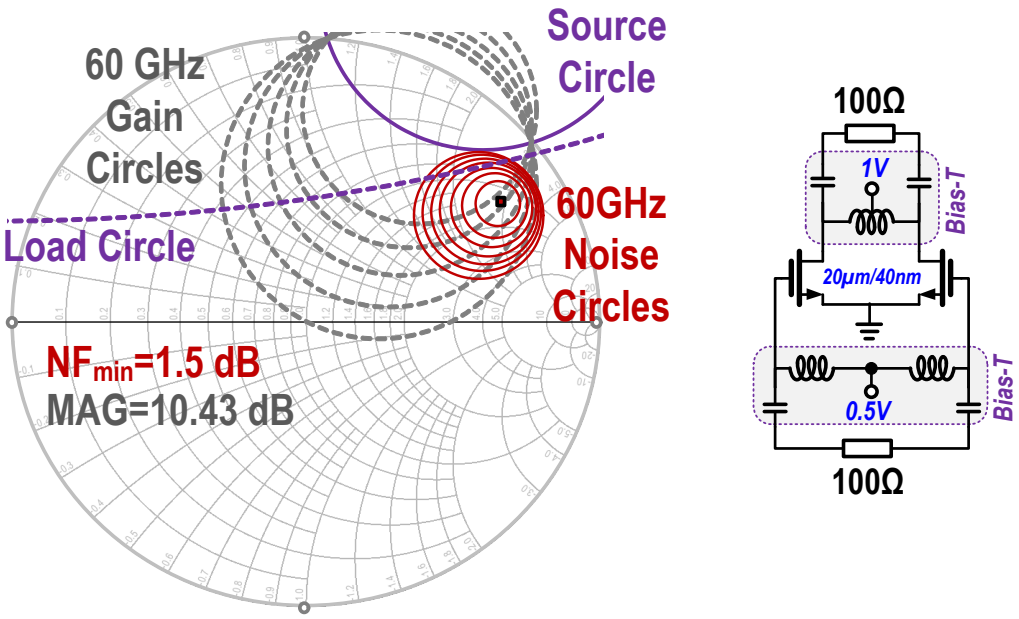
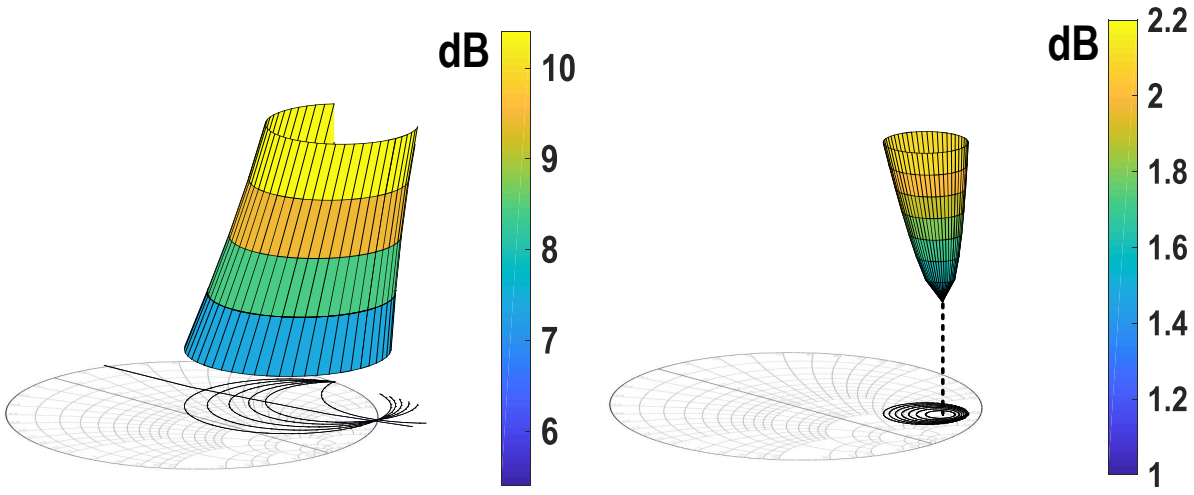


Figure 6.4: Noise, gain, source stability, load stability circles at 60 GHz of a 20-μm wide FB-NFET device



(a) (b)

Figure 6.5: 3D projection of (a) gain circles (b) noise circles at 60 GHz of a 20-μm wide FB-NFET device

(MAG) remain constant. A bigger circle means that the corresponding impedances realize a constant larger NF and lower MAG. The minimum noise figure of the transistor is 1.5 dB at 60 GHz with a Z_{opt} of 63.4+j147.2 (Ω) (see Fig. 6.4), which is insensitive to transistor scaling assuming constant bias current. Each larger circle with impedances moving away from Z_{opt} corresponds to an increase in the device noise figure with 0.1 dB steps. The MAG of the transistor is 10.43 dB at 60 GHz and the MAG contour is the smallest dotted circle shown in Fig. 6.4. Larger circles correspond to a decrease in the gain in steps of 1 dB. Usually, Z_{opt} doesn't necessarily fall on the MAG circle [80]. However, the simulations show that they are very close in this case. As a result, matching to Z_{opt} also realizes a power gain close to MAG of the transistor. Furthermore, source and load stability circles (i.e., circles defining source and load impedances that realize unstable and stable amplification) are plotted showing the impedance range that corresponds to stable amplification. Of course, any impedance outside the smith chart has a negative resistance which is impractical to implement using passive components, thus any impedance value outside both source and load circles and inside the smith chart maintains a stable amplifier. A 3D projection of both noise and gain circles is shown in Fig. 6.5. The noise circles are plotted from NF_{min} up to 2.2 dB in 0.1 dB steps. The gain circles are drawn from MAG down to 6.43 dB in 1 dB steps.

It should be noted that a device dimensions of 20μm/1μm is chosen to limit the DC power consumption, especially for a differential LNA that uses 2 devices in each stage of amplification. Moreover, the interconnect capacitance added by BEOL parasitics helps in reducing the size of the tuning inductor required for matching, thus reducing the noise figure contribution (i.e., lower resistive losses) by reducing the inductor's winding unfolded length. The DC power consumption of one differential stage biased at V_{GS} = 0.5 V and V_{DS} = 1 V is 10.8 mW, so a 2-stage amplifier requirement consumes 21.6 mW.

6.2.2 2-Stage Common-Source Amplifier Schematic

In this work, a 2-stage amplifier design is developed for handset applications. Careful impedance matching should be performed to achieve peak performance (i.e., NF≈1.5 dB and G≈10.43 dB per one stage) from active and passive components of the amplifier. Fig. 6.6 shows the schematic of the proposed 60-GHz LNA developed in this work. Each stage consists of a common-source differential amplifier with feedback capacitors (C_{N1}, C_{N2}) to compensate for reduced forward gain due to the Miller effect (i.e., C_{gd} feedback) by setting $C_N = -C_{gd}$. If C_N exceeds -C_{gd}, the amplifier's stability factor decreases and approach unity.

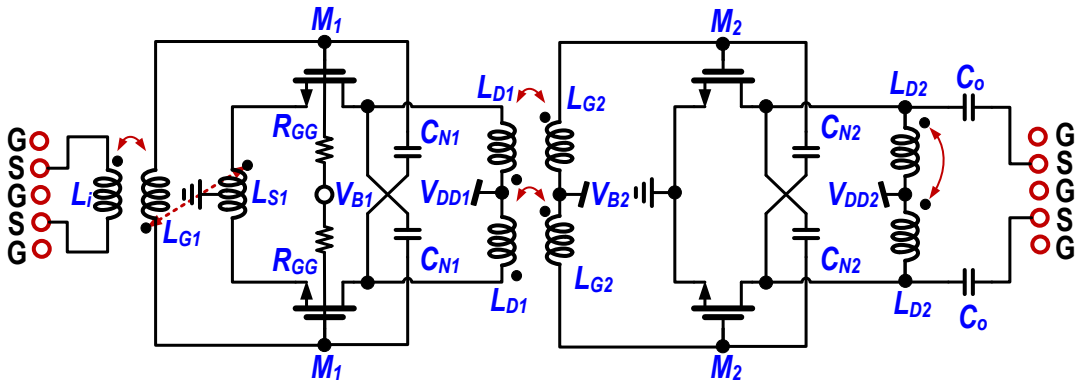


Figure 6.6: 2-stage low-noise amplifier schematic

For stand-alone LNA characterization, input and output port impedances are matched to 100 Ω differentially. The amplifier has 3 matching networks. The input matching network consists of 3 transformer windings: L_i, L_{G1}, and L_{S1}. Windings L_i and L_{G1} transform 100 Ω to the signal source impedance of both noise and gain matching at 60 GHz. Technically, the NFET is sized to set $Re\{Z_{opt}\}$ to 100 Ω. However, due to the impedance shifts caused by BEOL RC parasitic networks, the transformer turns ratio is set to 1:1.53 (i.e., not exactly 1:1). Winding L_s is used as a source degeneration inductor to boost $Re\{Z_{in}\}$ to 100Ω for power matching. However, the amplifier gain decreases when degeneration is added. By coupling L_{S1} to L_{G1}, wide-band matching and reduced transformer losses can be realized [58] (i.e., transformer feedback between L_{G1} and L_{S1}).

The inter-stage step-up transformer (L_{D1},L_{G2}) performs noise matching to the second stage. Moreover, it allows DC bias isolation between the two stages of the LNA. Several efforts were made to simultaneously noise and power match the first stage to the second stage by adding a source degeneration inductor. However, since the target bandwidth is 6-7 GHz, source degeneration for the second stage can be neglected. The output matching network is a lumped LC network that transforms the capacitive impedance seen by the output stage to 100 Ω.

Both amplifier stages are biased at $V_{GS} = 0.5$ V and $V_{DS} = 1$ V. The first stage gate bias is driven by a poly-silicon resistor R_{GG} of 25 kΩ for each device. The other DC biasing nodes are the AC ground nodes of the corresponding transformer windings.

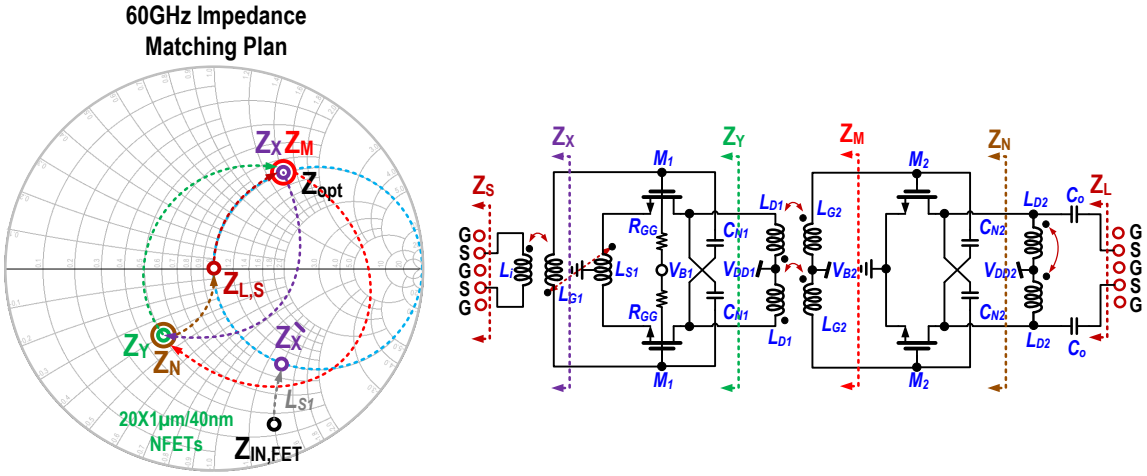


Figure 6.7: 60-GHz impedance matching plan for the low-noise amplifier

6.2.3 Impedance Matching Plan

Fig. 6.7 summarizes the impedance matching across different amplifier components from source to load. The input port impedance Z_L starts from the Smith chart center at 100 Ω. The input matching network moves Z_S to Z_X to simultaneously match it to Z_{opt} and $Z_X^{'}$, while L_{S1} degenerates the source terminal and moves $Z_{IN,FET}$ to $Z_X^{'}$. The output impedance of the first stage Z_Y is matched to Z_M by the inter-stage matching network. The output impedance of the second stage, Z_N is matched to a 100-Ω load, Z_L by a lumped LC matching network. Capacitor C_o blocks the supply voltage of the second stage from the output port.

6.2.4 Active/Passive Components Design

Fig. 6.8 shows the layout of the NFET. The device consists of 4 multiples of 5 interdigitated fingers each, where the finger width and length are 1 μm and 40 nm, respectively. The finger placement is aimed at minimizing the gate resistance of the device by creating a mesh network of gate fingers, and then creating a double contact for the mesh using the BEOL metal routing shown in Fig. 6.8. Simulations after parasitics are extracted for these devices predict a 0.15 to 0.2 dB reduction in the device NF_{min} compared to a layout comprised of 20 interdigitated finger. The differential pair use a feedback capacitor C_{N1} of 8 fF for the first stage, and C_{N2} of 15 fF for the second stage. The feedback capacitors are realized using the VNCAP kit model and implemented using the C1 metal layer.

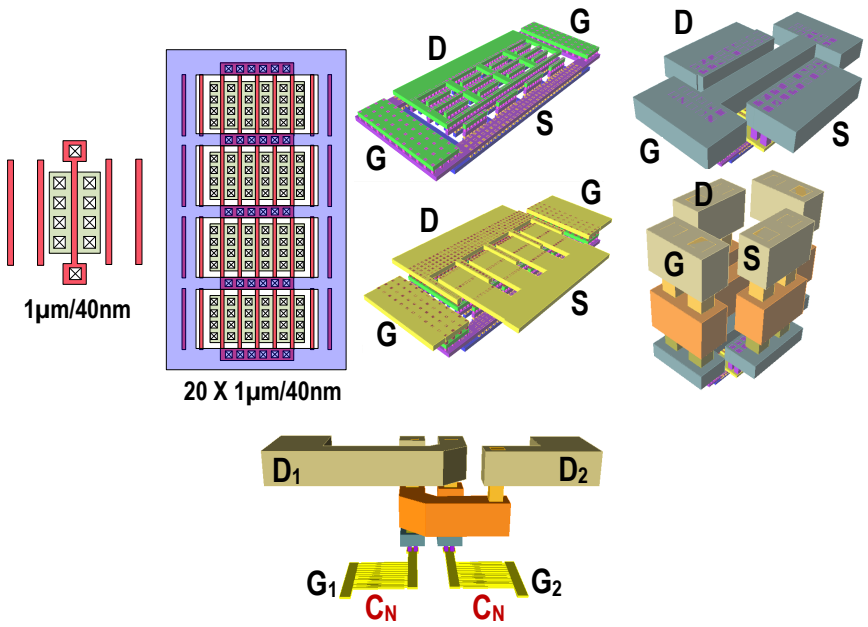


Figure 6.8: NFET common-source device and BEOL stack layout

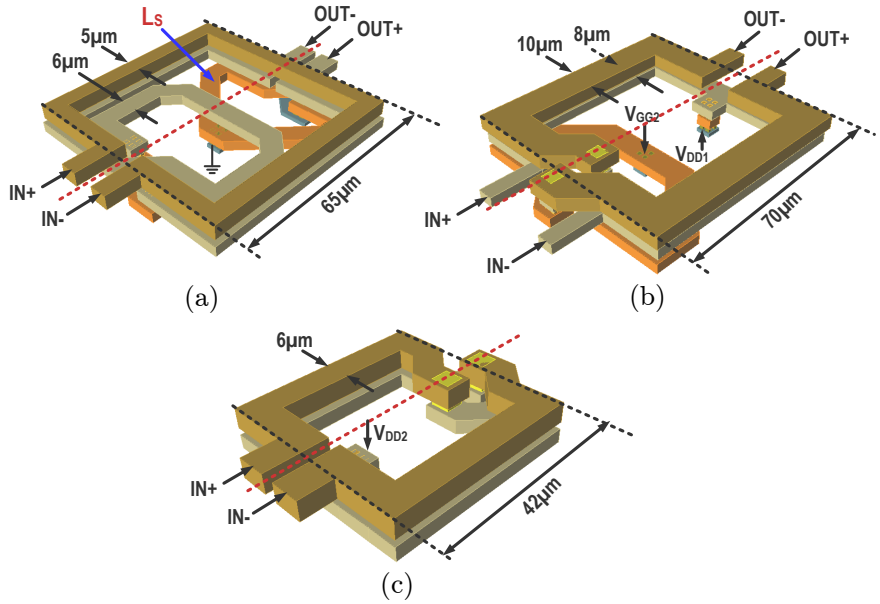


Figure 6.9: 3D projection of the transformers used for (a) input matching network (b) inter-stage matching network (c) output matching network

Table 6.1: Passive Component Design Parameters for the LNA

Element	Width	Outer dimensions	Inductance[1]	Capacitance	Coupling[1] factor (k)	Q @60G
L_i/L_{G1}	5μm/6μm	65μm×65μm	97.3/228pH	—	0.56	28.5
L_{G1}/L_{S1}	6μm	65μm×65μm	228/66pH	—	0.2	26.5/42
$2L_{D1}/2L_{G2}$	10μm/8μm	70μm×70μm	118.5/192pH	—	0.6	25.4/26.3
$2L_{D2}$	6μm	42μm×42μm	173pH	—	—	31
C_{N1}	—	5.4μm×6.5μm	—	8fF	—	256
C_{N2}	—	7μm×9.4μm	—	15fF	—	120
C_o	—	5μm×20μm	—	40fF	—	548

[1] Simulated at 1MHz frequency where capacitive coupling is negligible

Fig. 6.9 shows different physical layout configurations of the transformers developed in this work. The input transformer adopts stacking of the top 3 metal layers OA, OB, and LD, as shown in Fig. 6.9a. Winding L_i is implemented on the LD layer with 5-μm width and has a 65-μm outer dimension, while winding L_{G1} is implemented on the OB metal layer with a width of 6 μm. The degeneration inductor L_{S1} is realized using the OA layer, and it is directly coupled to L_{G1}. The interstage transformer design, which uses metal stacking is shown in Fig. 6.9b. Winding L_{D1} is realized using the OB metal of 8-μm width and has an outer dimension of 70 μm. Winding L_{G2} is implemented using layers OA and LD with 10-μm width and 70-μm outer dimension. The output transformer, shown in Fig. 6.9c, is realized by stacking 6-μm wide OB and LD metals with 42-μm outer dimension. All transformers are driven differentially, and biasing nodes are at virtual grounds due to layout symmetry. Table 6.1 summarizes the performance of the passive components used in the design of the LNA.

6.2.5 Fabricated Prototype Layout

A die photo of the fabricated prototype is shown in Fig. 6.10. The 8-metal BEOL stack (Option 18) in 45-nm RF-SOI CMOS technology is used. The input and output ports of the LNA are matched to 50 Ω at each terminal. RF signal to each port is fed by 50-Ω microstrip transmission lines from the RF probe pads. The 50-Ω lines are designed using the 4.125-μm thick top metal (LD layer) for the RF signal and the C1 layer for the slotted

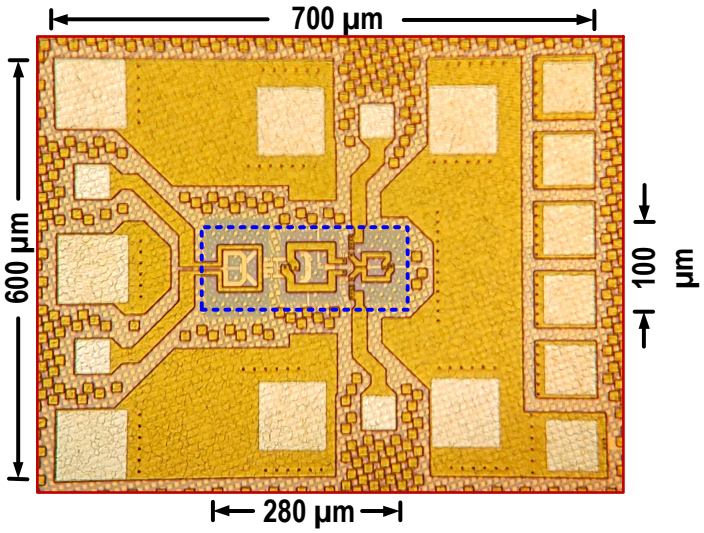


Figure 6.10: Die photo of the fabricated low-noise amplifier

ground plane. The total active area for the LNA is 0.028 mm^2.

6.3 Simulation Results

Forward power gain (i.e., $|S_{21}|$) and input-referred noise figure (NF) are plotted in Fig. 6.11. A minimum NF of 3.07 dB at 61 GHz and a maximum power gain of 20.8 dB at 60 GHz are predicted from simulations. A -3 dB gain bandwidth of 5.8 GHz is predicted between 57.2 GHz and 63 GHz. The corresponding NF values at the band edges are 3.6 dB and 3.23 dB, respectively.

Input/output return loss (RL) and reverse gain are plotted in Fig. 6.12. The LNA is wideband matched for 10-dB input RL across 9.2-GHz bandwidth from 57.8 GHz to 67 GHz, and 10-dB output RL across 11.2-GHz bandwidth from 53.6 GHz to 64.8 GHz.

Fig. 6.13 shows the trade-off between gain, NF, and DC power consumption across different supply voltages. The maximum allowed supply (i.e., transistor V_{DS}) in the 45-nm technology is 1 V. The optimized gain and NF achieved, 20.8 dB and 3.1 dB, respectively, at 1 V with a total power consumption of 21 mW. A 0.75 V supply decreases DC power to 12 mW (i.e., almost 50%) while degrading the gain by 1 dB and noise figure by 0.13 dB. The lower supply bound of 0.5 V further minimizes the power consumed to 5.9 mW, however, the gain and noise figure degrade by 3.2 dB and 0.42 dB, respectively.

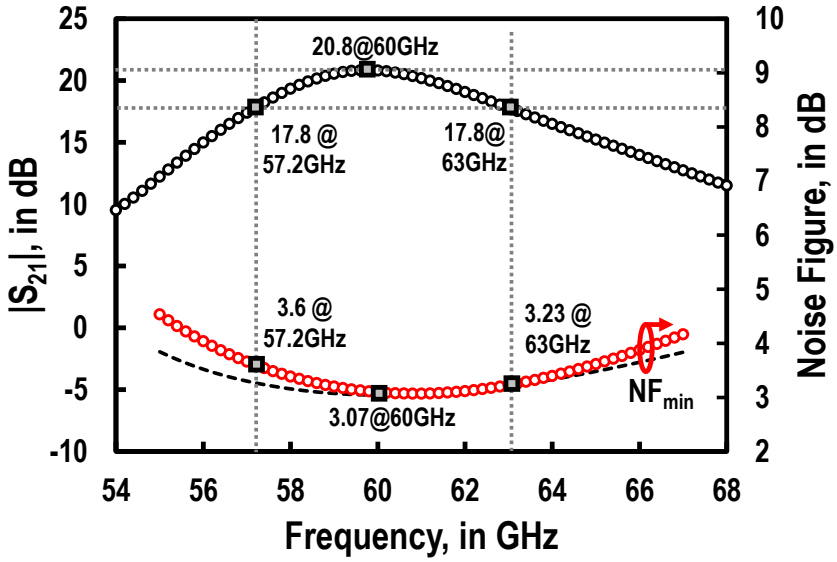


Figure 6.11: Small-signal gain and noise figure simulation results

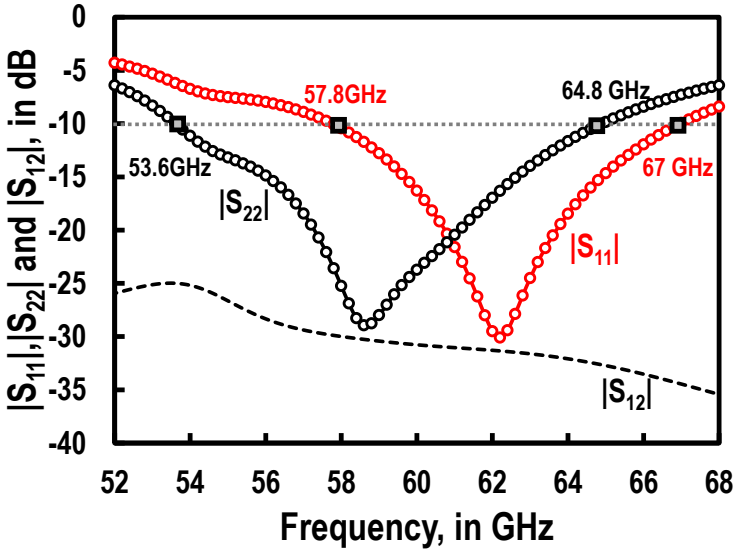
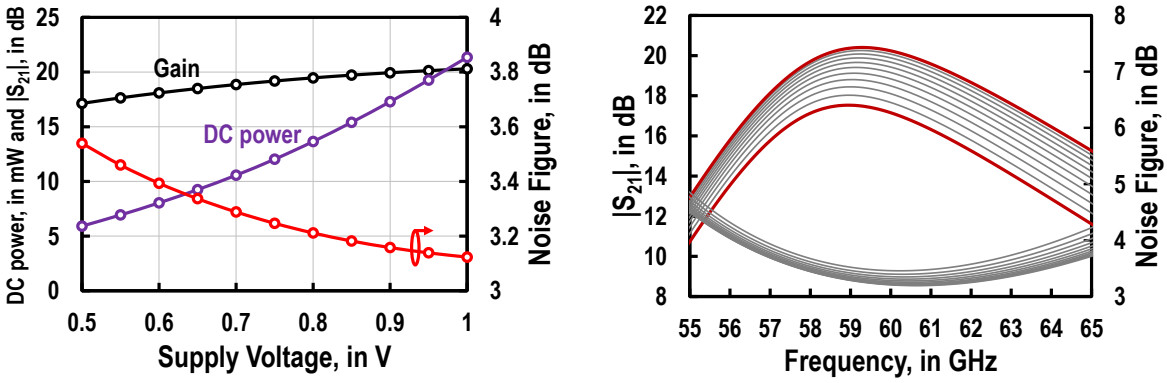


Figure 6.12: Input and output return loss small-signal simulation results



(a) (b)

Figure 6.13: Small-signal supply voltage sweep simulations (a) $|S_{21}|$, NF, and DC power consumption (b) $|S_{21}|$ and NF across frequency

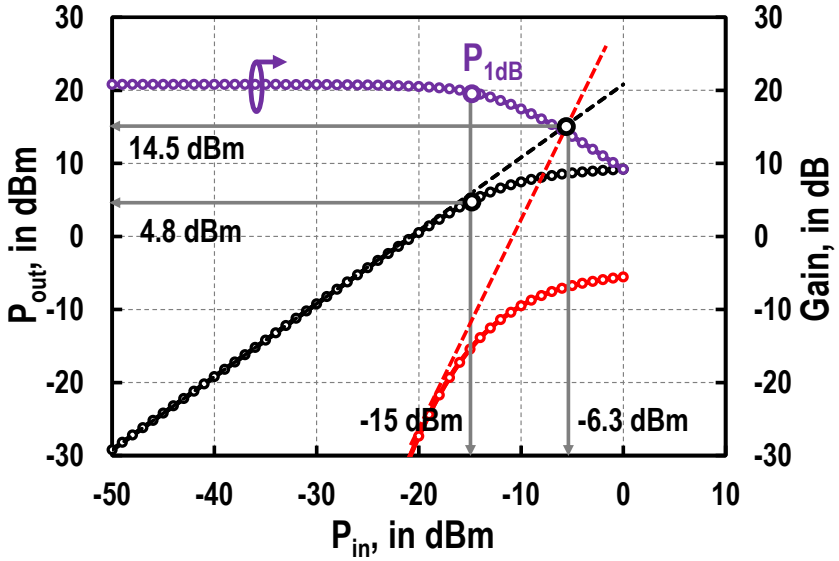


Figure 6.14: Large-signal linearity simulation results

The advantage of having a variable gain control is clear when integrating the LNA with a passive phase shifter (see Chapter 5 for the phase shifter design). The design target for the reconfigurable receiver chain is to compensate for any gain variation that arises when changing phase shift states. Since the proposed phase shifter achieves a 2-dB gain deviation, supply sweep simulations predict that supply level adjustments (i.e, 0.5 V to 1

V) are sufficient to vary the LNA gain and compensate for such deviation.

Large-signal simulation results are presented in Fig. 6.14. The output power for 1-dB gain compression OP_{1dB} is 4.8 dBm, which corresponds to an IP_{1dB} of -15 dBm. The third-order intercept point (OIP3) is 14.5 dBm, or -6.3 dBm IIP3. It is expected that OP_{1dB} and OIP3 are lower than that predicted in Fig. 6.14 for reduced supply values.

Process variations are simulated using Monte Carlo simulations. The results are reported for 500 samples at 60 GHz. The average gain is 20.7 dB with a variation of ±1 dB and a standard deviation of 0.3 dB. The average noise figure is 3.12 dB with a variation of ±0.2 dB and a standard deviation of 0.06 dB. Supply variations are carried by simulating the design by varying the supply voltage with ±5%. The variation in gain and noise figure at 60 GHz in response to supply variation is ±0.27 dB and ±0.005 dB, respectively. Changing the simulation temperature from 0°C to 85°C predicts gain and noise figure variations to be 0.66 dB and 0.5 dB, respectively.

6.4 Literature Comparison

Table 6.2 shows a performance comparison between the proposed LNA design and other designs from the recent literature. The LNA is wideband matched from 57.8 GHz to 67 GHz (i.e., 15.3% fractional bandwidth) with a simulated return loss of larger than 10 dB. The proposed LNA bandwidth is comparable to that of the other LNAs listed. However, each wireless standard requires minimum fractional bandwidth (i.e., 11.6% for the 60-GHz band from 57 GHz to 64 GHz). The maximum simulated forward power gain of the proposed LNA is 20.8 dB biased at a current density of 270 μA/μm per stage, with a -3 dB bandwidth of 5.8 GHz across 57.2 to 63 GHz. The power gain of the LNA is larger than that in [23], which achieves a gain of 12.5 dB using single-ended 2-stage cascode topology with transmission line matching using 45-nm SOI-CMOS in the 60-GHz band. The gain of the proposed LNA is smaller than the differential 3-stage common-source LNA of [61] by 3 dB, which is biased at a lower current density of 100 μA/μm and realizes a higher minimum noise figure of 4 dB. The simulated minimum noise figure for the proposed LNA is 3.07 dB at 60 GHz, and the noise figure is less than 3.5 dB between 57.6 GHz and 64.6 GHz. This noise figure performance predicts a state-of-the-art in the 60-GHz band compared to [23,61] for multistage amplification, which realizes a noise figure of 4 dB each. The simulated OP_{1dB} is 4.8 dBm, which is the highest among the designs listed in the table. However, it is highly dependent on the supply voltage and the number of devices in cascode in the LNA core. The proposed LNA consumes 21 mW from the 1-V supply, which is higher than the designs listed in Table 6.2, especially the designs in [23] and [61]

that consumes 15 mW and 8 mW at 60 GHz, respectively. However, the DC power of the proposed LNA can be reduced to 12 mW, while maintaining a gain of 19.8 dB, and a noise figure of 3.2 dB. The proposed LNA occupies a compact physical area of 0.028 mm^2, which is the smallest among the designs listed in the table.

6.5 Conclusion

A fully-differential, wideband, 60-GHz 2-stage common-source LNA is developed in 45-nm SOI-CMOS using BEOL metal stack 18. The amplifier is wideband matched from 57.8 GHz to 67 GHz. The simulated maximum forward power gain is 20.8 dB. The minimum noise figure is 3.07 dB. The LNA realizes an OP_{1dB} of 4.8 dBm and consumes 21 mW from the 1-V supply. The LNA occupies a physical area of 0.028 mm^2.

Table 6.2: Performance Comparison with different mm-Wave LNAs from Recent Literature

	[59]	[62]	[23]	[23]	[23]	[61]	This Work(Sim.)
Tech.	45nm-SOI CMOS	45nm-SOI CMOS	45nm-SOI CMOS	45nm-SOI CMOS	45nm-SOI CMOS	65nm CMOS	45nm-SOI CMOS
Topology	2-Stage Cascode	2-Stage CS/Cascode	2-Stage Cascode	2-Stage Cascode	3-Stage Common Source	3-Stage Common Source	2-Stage Diff.Common Source
Freq. (GHz) [S_{11}<-10dB]	42.5-55	19-30	43-57	58-80	84-88	63-67	57.8-67
Gain (dB) [-3dB-BW(GHz)]	18.5 (43-53)	19.5 (16-24)	15 (40-53)	12.5 (60-73)	13.5 (76-88)	23 (57-64)	20.8 (57.2-63)
Noise Figure (dB)	2.9@47G	2@19G	3.3@45G	4@65G	5.7@85G	4	3.07@60G
Output P_{1dB} (dBm)	3	0	1.5	-2	-1.5	-3.5	4.8
Supply Voltage (V)	1.2	1/1.5	1.3	1.3	1	1.25	1
DC Power (mW)	22.8	32.5	20.8	15	13.5	8	21
Active Area (mm^2)	0.14	0.15	—	—	—	0.05	0.028

Chapter 7

CMOS 60 GHz Receiver Front-End Design

7.1 Introduction

This chapter proposes a scenario for the integration of a reconfigurable receiver front-end that can be scaled to create a phased-array receiver. The front-end consists of a cascaded SPDT switch, LNA, SPDT switch, and a phase shifter. The scope of this study is to predict the system performance from small-signal and large-signal simulations. Moreover, the physical layout of the front-end is highlighted to predict the overall area of a phased-array implementation with increasing array order.

In an array configuration, each receiver front-end slice is combined using a passive, on-chip power combiner. A 4-to-1 Wilkinson-type power combiner is used to realize this function. Based on the array expansion study introduced in Chapter 3, a 2×2 phased-array order is selected to minimize the system loss/phase mismatch when interfacing with off-chip antennas via packaging.

7.2 Reconfigurable Receive Front-End Design

Fig. 7.1 shows the schematic design of the proposed system. The system consists of cascading the building blocks developed in the design chapters of this work. SPDT switches, a 2-stage LNA, and a phase shifter are cascaded to realize a reconfigurable receiver slice.

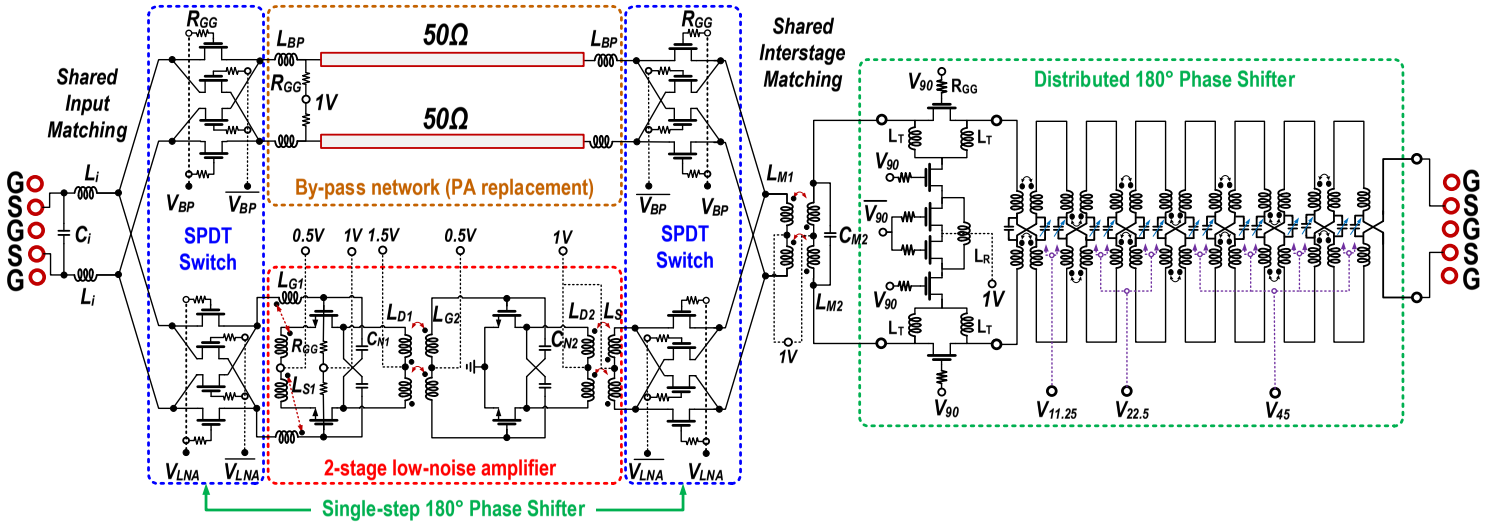


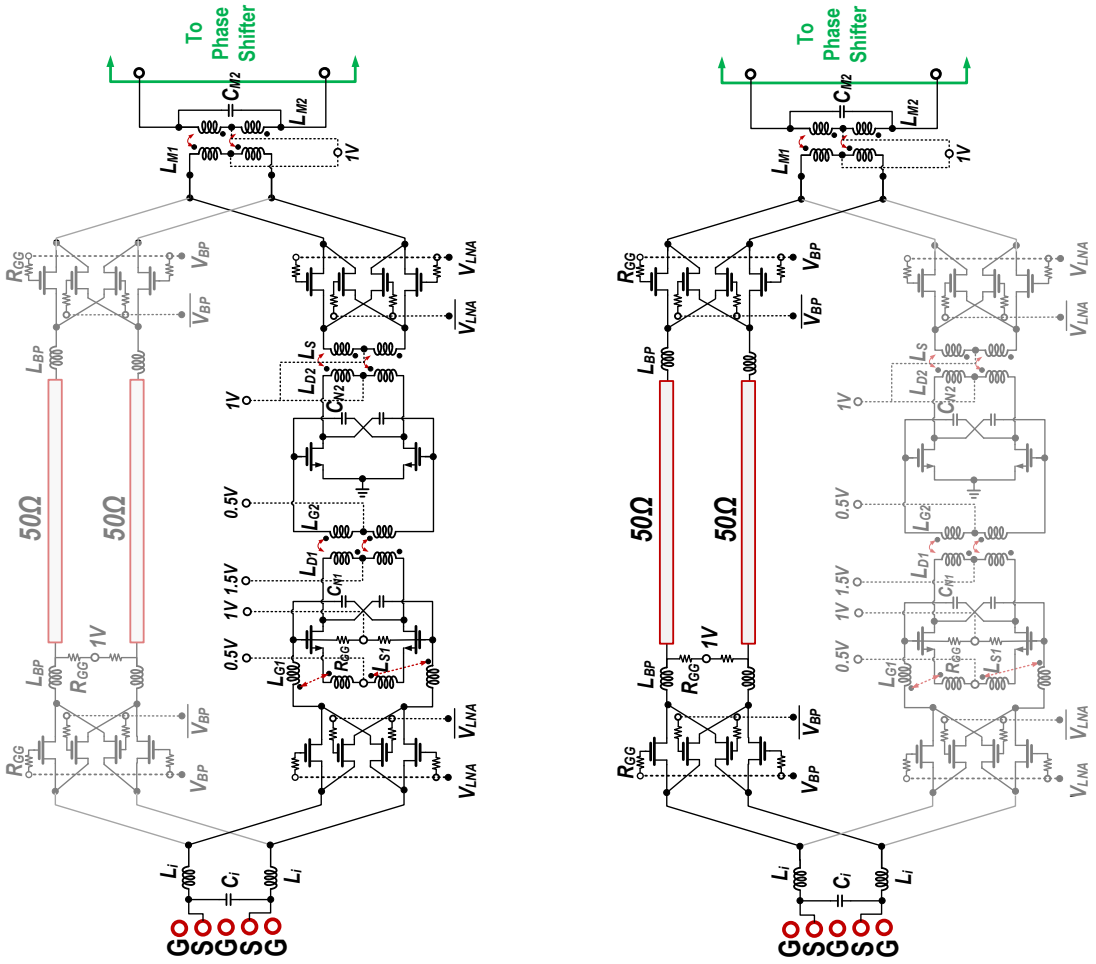
Figure 7.1: Schematic design of the 60-GHz receiver front-end system integration. The system consists of a cascaded SPDT switch, a 2-stage low-noise amplifier, SPDT switch and a phase shifter.

For characterization, the power amplifier in the transmit path is replaced with a by-pass network to model the RF losses. This network consists of matching inductors L_{BP} and 50-Ω transmission lines as shown in Fig. 7.1. The phase shifter design is reduced to distributed 180° states. A single 180° phase step is realized using one of the SPDT switches. Inter-stage transformer networks are used to perform impedance matching between cascaded components. Losses of all components that appear prior to the LNA in the RF path leading from the antenna add directly to the overall noise figure. As a result, impedance matching using series inductors is adopted to minimize insertion loss and improve noise figure. Furthermore, the input port matching network losses via L_i and C_i add to the overall noise figure and should be minimized. The input SPDT switch is matched to the LNA using inductor L_{G1}.

To improve the linearity of both SPDT switches, especially in the transmit mode, the signal lines are biased at 1 V through the gate terminal of the LNA first stage as shown in Fig. 7.1. Since the common-source devices of the LNA are biased for NF_{min}, V_{GS} is set to 0.5 V. As a result, the source terminal of the differential amplifier is biased to 0.5 V instead of 0 V (i.e., ground terminal). The voltage V_{DS} is set to 1 V by biasing the inductor-tap for transformer winding L_{D1} to 1.5V. The second stage output of the LNA is matched to the second SPDT switch using a fully differential transformer (i.e., using L_{D2} and L_S). The common port of the second SPDT switch is then matched to the phase shifter (i.e., with 100 Ω input/output ports) via differential transformer L_{M1} and L_{M2} and shunt capacitor C_{M2}.

7.2.1 Modes of Operation

Fig. 7.2 shows the two operating modes of the receiver front-end system used for characterization in simulation. Fig. 7.2a shows the receive mode, where the LNA path is activated. This is achieved by turning OFF the by-pass network switches at both input/phase shifter ports, and turning ON the LNA path switches at the same ports. This allows the received RF signal to travel through the LNA and the phase shifter. The by-pass mode is activated by turning ON the by-pass network switches and turning OFF the LNA path switches as shown in Fig. 7.2b. As a result, the input RF signal flows through a purely passive network, including the phase shifter, to the output port. This mode is useful to characterize the total insertion loss between the receiver ports.



(a) (b)

Figure 7.2: Receiver front-end operation modes (phase shifter not shown) (a) receive mode (b) by-pass mode

7.2.2 Simulation Results

A fabrication-ready layout of the reconfigurable front-end is shown in Fig. 7.3. The input and output ports of the LNA are all matched to 50 Ω. RF signal to each port is fed via 50-Ω microstrip transmission lines from RF probe pads. The 50-Ω lines are designed using the 4.125 μm thick top metal (LD layer) for the RF signal path and C1 layer for the perforated ground plane. The 8-metal BEOL stack (Option 18) in the 45-nm RF-SOI

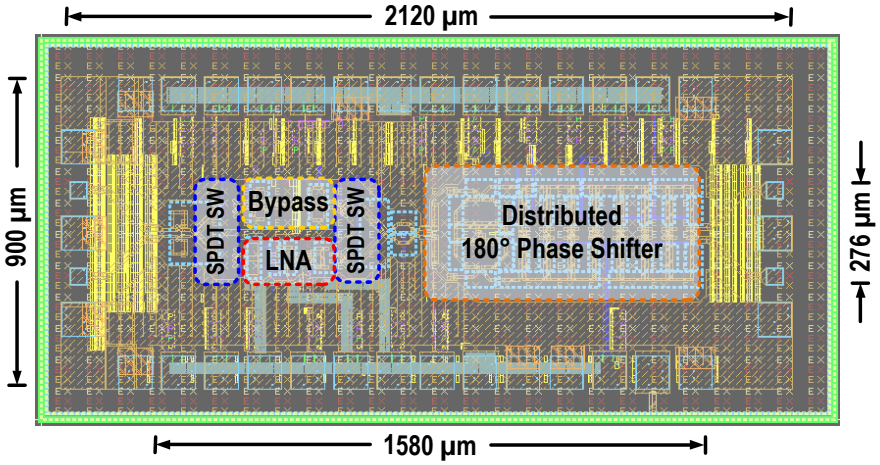


Figure 7.3: Fabrication-ready layout of the reconfigurable receiver front-end

CMOS technology is used. The total area for the receiver front-end, excluding probe pads and feeding lines, is 0.436 mm^2. The total DC power consumption is determined primarily by the LNA, which consumes less than 22 mW from the 1-V supply.

Differential small-signal simulations are shown in Fig. 7.4. Both input and output ports are matched to 100 Ω with return loss larger than 10 dB between 55 and 65 GHz band across all phase shift states. The simulated forward gain of the receiver front-end is 9.8 dB at 61 GHz and varies by ±1 dB across all phase states. This small change could be accommodated by adding a dedicated variable-gain amplifier (VGA) for gain adjustments. Another solution is to design the LNA with variable gain control. The reverse isolation of the receiver front-end is better than 35 dB over the entire 55 to 65 GHz band, from simulations.

Noise figure (NF) simulations are plotted in Fig. 7.5. The simulated minimum NF is 5.9 dB at 62.5 GHz with 0.25 dB NF deviation across phase shift states. The NF remains below 6.5 dB from 59 GHz up to 64.5 GHz. Since the variation in phase shifter insertion loss (IL) is within 2 to 3 dB, it has little to no effect on the overall NF deviation. However, the noise power produced by the LNA and the input SPDT switch directly affects the overall noise figure, and therefore it is necessary to keep them as low as possible.

Fig. 7.6 shows the simulated phase shift of the forward gain across all phase states. The receiver front-end maintains 360° phase steering with 11.25° phase steps. As mentioned previously, the phase shift is distributed through a single-step 90° phase shifter and a slow-wave 90° phase shifter, while the single-step 180° phase shift is implemented by one of the differential SPDT switches. This partitioning reduces the IL of the phase shifter.

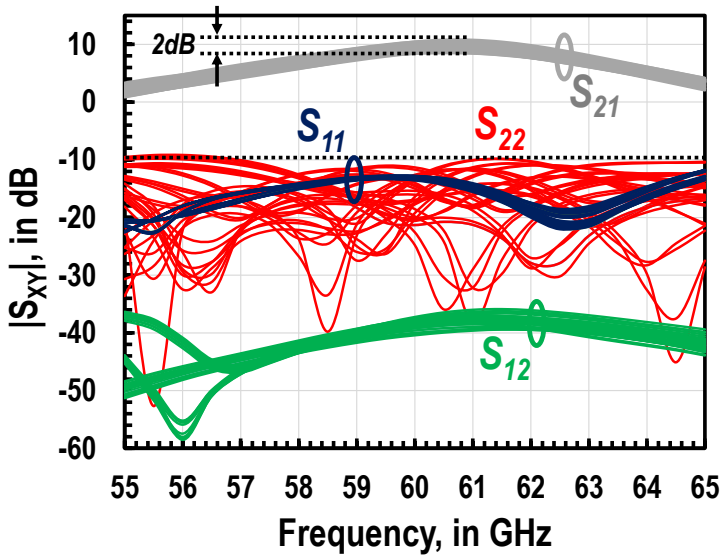


Figure 7.4: Small-signal S-parameters simulation results of the complete receiver across all phase states

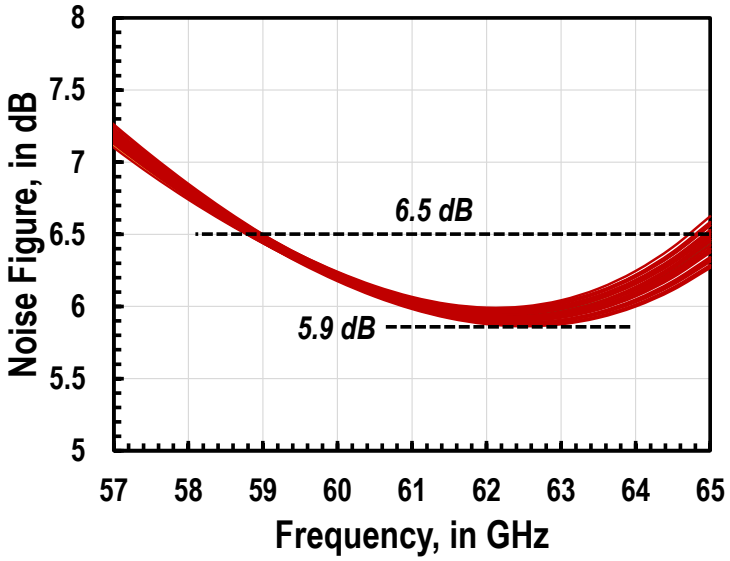


Figure 7.5: Noise figure simulations results across all phase states

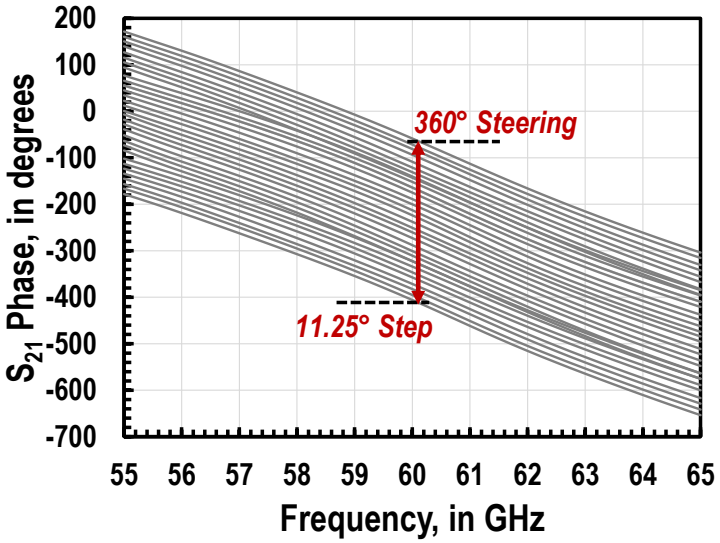


Figure 7.6: Receiver insertion phase response across all phase states

Fig. 7.7 shows the receiver insertion loss simulated in the by-pass mode. The average insertion loss of the port-to-port passive network is 9.85 dB at 60 GHz and varies by ±1.15 dB. The magnitude of the insertion loss remains almost flat from 57 GHz to 63 GHz. As a result, gain flatness in the receive mode is dependent on the flatness of the low-noise amplifier gain across the same frequency band.

Large-signal simulation results of the receive mode at 60 GHz are plotted in Fig. 7.8. The predicted input (IP_{1dB}) and output (OP_{1dB}) 1-dB compression points for the receiver are -9.5 dBm and 2.5 dBm, respectively. These results are far above the received power levels across the 60-GHz band (i.e., smaller than -60 dBm). It should be noted that the large-signal compression performance is limited by the low-noise amplifier. For a complete transceiver in the transmit mode, the large-signal performance is expected to be limited by the SPDT switches (i.e., $\approx$ 20 dBm).

Process variations are simulated using Monte Carlo simulations. The results are reported for 500 samples at 60 GHz. The average total gain is 10.8 dB with a variation of ±1.4 dB and a standard deviation of 0.4 dB. The average total noise figure is 6.3 dB with a variation of ±0.3 dB and a standard deviation of 0.1 dB. Supply variations are carried by simulating the design by varying the supply voltage with ±5%. The variation in gain and noise figure at 60 GHz in response to supply variation is ±0.43 dB and ±0.15 dB, respectively. Changing the simulation temperature from 0°C to 85°C predicts gain and noise figure variations to be 1.2 dB and 0.9 dB, respectively.

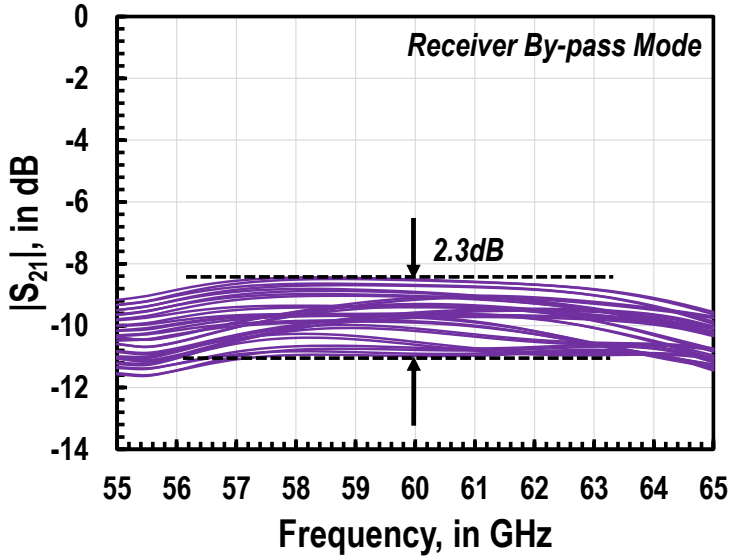


Figure 7.7: Receiver by-pass insertion loss across all phase states

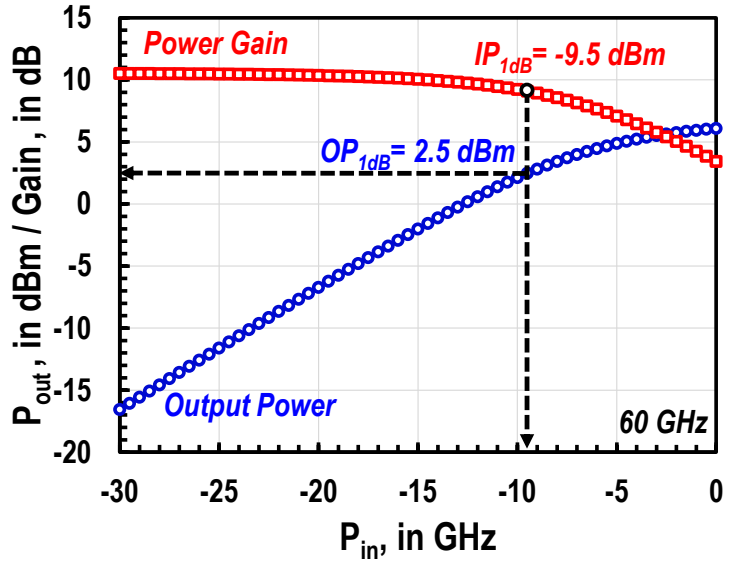


Figure 7.8: Large-signal simulation results at 60 GHz

Chapter 8

Contributions and Future Work

This chapter summarizes the contributions of the Ph.D. thesis project to individual RFIC circuit design as well as system integration and characterization. Furthermore, recommendations for future research in these areas are proposed.

8.1 Contribution

This dissertation has focused on the analysis, design, and validation of CMOS receiver front-end components suitable for 60-GHz phased-antenna-array radios for portable wireless handset applications. The main building blocks developed for a reconfigurable receiver include: 1) a single-pole, single-throw (SPST) switch, 2) a single-pole, double-throw (SPDT) switch, 3) a low-noise amplifier (LNA) and 4) a phase shifter (PS). The proposed reconfigurable receiver front-end is comprised of an SPDT switch, LNA, a second SPDT switch, and the phase shifter in cascade. All circuit designs are fully-differential for ease of integration onto a single silicon chip. The circuit prototypes are implemented in GlobalFoundaries 45-nm RF SOI-CMOS using BEOL stack options 8 and 18, which is a technology developed primarily for mm-wave applications.

The proposed SPST switch realizes state-of-the-art port-to-port isolation of better than 50 dB from DC to 43.5 GHz while maintaining an insertion loss below 3 dB over the entire band. The prototype realizes large-signal compression (IP_{1dB}) of 19.6 dBm when the switch is driven differentially. The circuit occupies an active area of 0.0058 mm^2 in 45-nm SOI-CMOS (13.5-Ω.cm resistivity). The proposed switch isolation is better by at least 12 dB than the highest reported in [41] at the 60-GHz band and [75] at the 28-GHz band.

Furthermore, the switch IP_{1dB} is larger by at least 10 dB than the highest reported at the 60-GHz band in [74] and [72].

Based on the SPST switch concept, the 60-GHz SPDT switch is comprised of two SPST switch instances with the outputs combined via a balun. At the receiver input, the balun is connected to a single-ended antenna port. Both LNA and PA ports are differential. The SPDT switch achieves a simulated, wideband, isolation of larger than 40 dB across the 55 to 65 GHz band, and the simulated insertion loss is maintained below 3.5 dB across the frequency band. The fabricated prototype occupies an active area of 0.117 mm^2 in 45-nm SOI-CMOS. The simulated isolation is larger than the highest reported in [38] and [41] at the 60-GHz band. The IP_{1dB} (i.e., 21 dBm) is predicted to be larger by at least 6 dB from the highest reported in [37] in the 60-GHz band.

The fully-differential, passive 360° phase shifter proposed in this thesis consists of a 90° switched-LC network, a distributed switched-C network based on a slow-wave artificial transmission line, and a phase inverter. The phase shifter is digitally controlled, and the prototype has a phase resolution of 11.25°. The simulated average insertion loss is 5.3 dB with a simulated rms IL error of less than 1 dB over the 55 to 65 GHz band. Moreover, the simulated average group delay is 61 ps with less than 4 ps rms error across 10 GHz bandwidth. The rms phase error is expected to be less than 7 ° across the full bandwidth. The simulated large-signal compression (IP_{1dB}) is 16 dBm when the phase shifter is driven differentially. The active area of the fabricated prototype is 0.245 mm^2 in 45-nm SOI-CMOS. The proposed phase shifter realizes smaller IL than the lowest reported in [47] at smaller phase resolution and smaller by 12 dB than the reported in [38] at the 60-GHz band. Furthermore, the simulated IP_{1dB} is larger than the highest reported in [40] by 4 dB.

A fully-differential LNA is developed at a center frequency of 60 GHz. The 2-stage design is comprised of common-source amplifiers with capacitive feedback for gain boosting. All transistors are biased at their current density for minimum noise figure contribution in a differential 100-Ω system. The simulated minimum noise figure is 3.07 dB and the maximum forward gain is 20.8 dB with a 3-dB bandwidth of 5.8 GHz. Both input and output ports are matched to 100-Ω with simulated larger than 10 dB input return loss between 57.8 and 67 GHz. The simulated -1 dB output compression point (OP_{1dB}) is 4.8 dBm, and the total DC power consumption is 21 mW from the 1-V supply. The fabricated prototype consumes an active area of 0.028 mm^2 in 45-nm SOI-CMOS. The simulated noise figure is smaller than the lowest reported in [61] and [23] at the 60-GHz band.

Moreover, this project has investigated the effects of system integration of different blocks on overall receiver performance. Small-signal simulations of a complete receiver

front-end predict input and output port matching with larger than 10-dB return loss across 55 GHz to 65 GHz band, a forward gain of 9.8 dB with ±1 dB gain deviation across all phase states. The simulated minimum noise figure is 5.9 dB at 62 GHz and remains below 6.5 dB from 59 GHz to 64 GHz. Large-signal simulations estimate the IP_{1dB} and the OP_{1dB} of -9.5 dBm and 2.5 dBm, respectively. A single-slice prototype consumes an active area of 0.436 mm^2

8.2 Future Work

During the circuit design and fabrication cycle, several potential research and development areas have been identified, which are summarized in this section. Firstly, on-chip calibration can be used for phase shifters to be able to maintain phase shift uniformity in terms of rms phase error across states after silicon fabrication. Moreover, it can be used to perform fine phase shift (i.e., less than 5°) control over the electronic beam of a phased-array transceiver. Furthermore, all front-end circuits can benefit from calibration against the process, voltage, and temperature performance variations. Another potential area to consider is to design switched-inductor networks with high-Q factor (i.e., larger than 20) at 60 GHz. This feature can be adopted with switched-capacitor networks to extend the phase shift range of a single repeatable cell using 2-bit control (i.e., 1-bit for switched-L and 1-bit for switched-C), which provides 4 phase states while maintaining Z_c close to 50 Ω. As a result, a 360° phase shift can be achieved using a fewer number of cells, which could potentially minimize IL further if properly designed.

Another research area to consider is to investigate circuit techniques to synthesize variable gain control for the low-noise amplifier in addition to gain calibration. calibration of gain and gain control is useful when compensating for the receiver losses and calibrating the receiver sensitivity based on the receiver power level.

Due to the continuous development of CMOS technologies for mm-wave applications, a logical step for the future development of this project is to port the designs to a more advanced technology node (e.g., 22-nm FDSOI) aiming for higher f_t and f_{max}. Moreover, greater silicon integration at a low cost is also predicted.

8.3 List of Publications

This section highlights the academic publications based on the contributions listed in Section 8.1.

Accepted/Submitted publications :

1. A. Eltaliawy, J. R. Long and N. Cahoon, "A DC to 43-GHz SPST Switch with Minimum 50-dB Isolation and +19.6-dBm Large-Signal Power Handling in 45-nm SOI-CMOS," *2020 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, Los Angeles, CA, USA, 2020, pp. 63-66 (Best paper award finalist)

2. A. Eltaliawy and J. R. Long, "A Broadband, mm-Wave SPST Switch with Minimum 50-dB Isolation in 45-nm SOI-CMOS," *2020 IEEE Transactions on Microwave Theory and Techniques*, (Invited special issue)

3. A. Eltaliawy and J. R. Long, "A Modified Noise Analysis and Design Flow of CMOS RF/mm-Wave Low-Noise Amplifiers for Wireless Applications," *2020 IEEE Transactions on Circuits and Systems I*, (Submitted)

Publications in preparation :

1. Conference/letter paper on the SPDT switch design

2. Conference/letter paper on the phase shifter design

3. Journal paper on the phase shifter design

4. Letter paper on the LNA design

5. Conference/letter paper on the receiver front-end design

6. Journal paper on the receiver front-end design

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APPENDICES

Appendix A

Array factor radiation pattern of linear antenna arrays

This matlab code aims at plotting and viewing the array factor radiation pattern of linear antenna arrays in 2D and 3D dimensions. The user can configure the following parameters in both x and y directions : the array order, normalized antenna separation to wave-length, antenna gain and linear antenna phase gradient.

```
clear all;
close all;

M=4; %array-order in x-direction
N=4; %array-order in y-direction

SX=[0.5 0.5 0.5]; % normalized antenna separation to lambda in x-direction
SY=[0.5 0.5 0.5]; % normalized antenna separation to lambda in y-direction

IX=[1 1 1 1]; % normalized antenna gain in x-direction
IY=[1 1 1 1]; % normalized antenna gain in y-direction

phase_deg_x=[0 30 60 90]; % linear antenna phase gradient in x-direction
phase_deg_y=[0 0 0 0]; % linear antenna phase gradient in y-direction

th_pts=200;
```

```
syms th ph;

phase_x = phase_deg_x .* (pi /180);
phase_y = phase_deg_y .* (pi /180);
AF=0;
DX=0;
DY=0;
for m=1:1:M
  for n=1:1:N
    AF=AF + (IX(m)*IY(n)*exp(j*((2*pi*DX*sin(th)*cos(ph))+phase_x(m)))
   *exp(j*((2*pi*DY*sin(th)*sin(ph))+phase_y(n))));
  % AF equation should be written in one line
    if n~=N
     DY=SY(n)+ DY
    end
  end
    if m~=M
     DX=SX(m)+ DX
     DY=0
    end
end

th_vtr=0:0.01:2*pi;
phi_deg=90
phi=phi_deg*pi/180

AF_abs=abs(AF);
AF_values_0=subs(AF_abs,{th,ph},{th_vtr,0});
AF_values_90=subs(AF_abs,{th,ph},{th_vtr,phi});
AF_max_0=max(AF_values_0);
AF_max_90=max(AF_values_0);

AF_norm_0=AF_abs/AF_max_0;
AF_norm_90=AF_abs/AF_max_90;

th_draw=linspace(-0.5*pi,0.5*pi,th_pts)
% theta range 0-->2*pi to double the number of points
AF_draw_0=(subs(10*log10(AF_norm_0),{th,ph},{th_draw,0}))
```

```
AF_draw_0_d=double(AF_draw_0)
AF_draw_90=subs(10*log10(AF_norm_90),{th,ph},{th_draw,phi})
AF_draw_90_d=double(AF_draw_90)

%2D plot:-
%---------
figure(1)
pol1=polaraxes
polarplot(pol1,th_draw(2:length(th_draw)),AF_draw_0(2:length(AF_draw_0)),'-B');
pol1.ThetaDir = 'clockwise';
pol1.ThetaZeroLocation = 'top';
rlim([-30 0])
title('F(theta) at phi=0');

figure(2)
pol2=polaraxes
polarplot(th_draw(2:length(th_draw)),AF_draw_90(2:length(AF_draw_90)),'-B');
pol2.ThetaDir = 'clockwise';
pol2.ThetaZeroLocation = 'top';
rlim([-30 0])
title('F(theta) at phi=90');


% 3D plot:-
%----------
M=100;
[phi,theta] = meshgrid(0:((2*pi)/M):2*pi,-pi/2:((pi)/M):pi/2);
th1=pi/2 -theta;
AF_draw_3d=subs(AF_norm_0,{th,ph},{th1,phi});
[x,y,z] = sph2cart(phi,theta,double(AF_draw_3d));
figure(3)
surf(x,y,z,'EdgeColor','none','FaceAlpha',1);
xlabel('x');
ylabel('y');
zlabel('z');
title('F(th,phi)');
zlim([0,1]);
```

Appendix B

ESD protection for DC pads

All fabricated prototypes have DC bias pads mounted on-chip for biasing control lines. These pads are wire-bonded to the chip package pads by leads. Due to human interaction, the electrostatic discharge (ESD) may damage the transistors connected to those DC pads during or after the wire-bonding process. As a result, each pad is protected against ESD by connecting the pad to the on-chip discharge network shown in Fig. B.1a.

The discharge loop consists of two diode networks as shown in Fig. B.1a. The first network consists of two reverse-biased diodes where node X is connected to the DC pad, the voltage applied to the DC pad shouldn't exceed the highest potential in the circuit which applied to node Y. The second network consists of an N cascaded forward-biased diodes where the overall turn-on voltage is equivalent to $N * V_{TH}$. The total turn-ON voltage should be greater than the voltage of node Y to prevent a short circuit current path to ground. Fig. B.1b shows an ESD example with an electrical surge event where the static charge induces a huge voltage spike to the pad. Assuming a V_{TH} of 0.6V for a single diode, the loop is closed when the voltage reaches 3V (i.e., $5*V_{TH}$) for ground discharging. ESD diode models are available with the process design kit as customized cells which can be easily used for building the ESD protection for each wire-bonded pad.

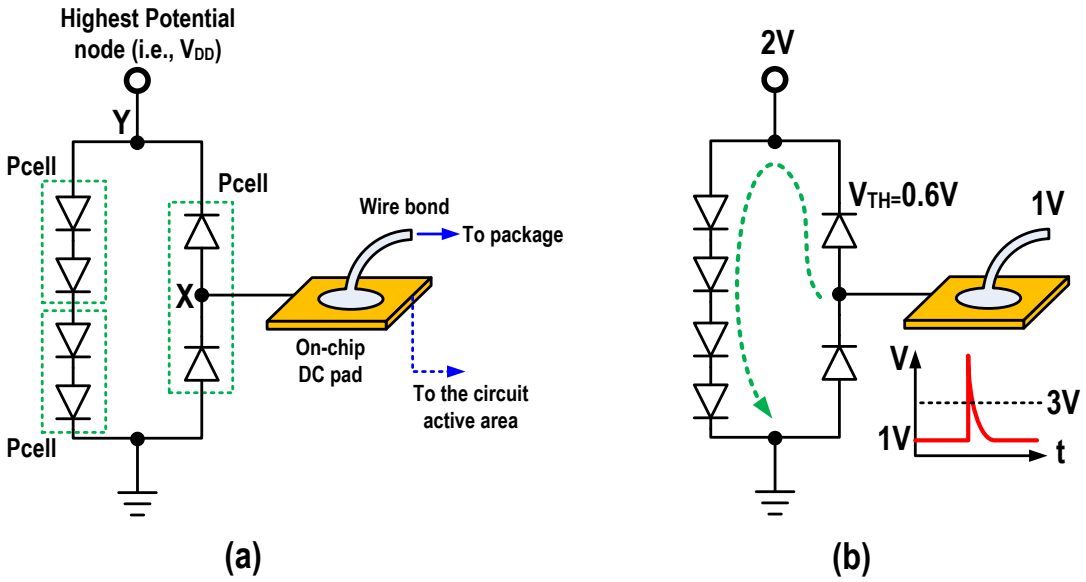

Figure B.1: ESD protection using diodes (a) circuit schematic (b) illustration of an ESD event